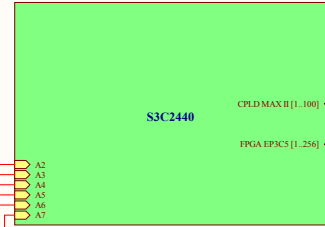
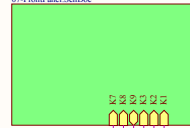


Hantek DSO5xxxB / DSO5xxxM - Tekway DST1xxxB DSO

PCB Layout Screenshot
99-PCB picture SchDoc

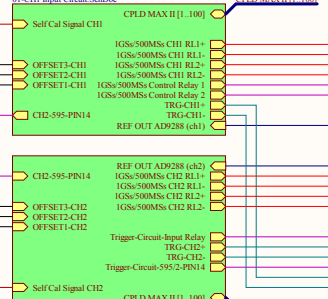


Front Panel
07-FrontPanel SchDoc

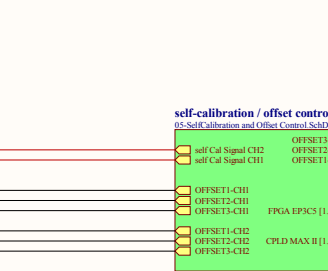


CPLD MAX II [1..100]
FPGA EP3K5 [1..256]

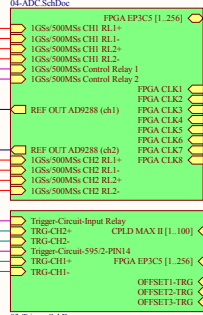
CH1 input
01-CH1 Input Circuit SchDoc



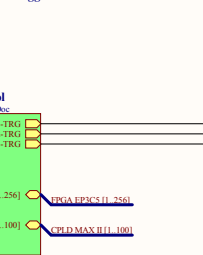
CH2 input
02-CH2 Input Circuit SchDoc



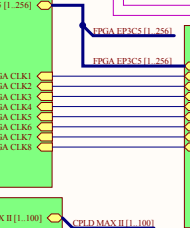
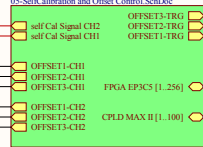
AD9288
04-ADC SchDoc



Trigger Circuit
03-Trigger SchDoc



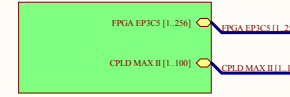
self-calibration / offset control
05-Self Calibration and Offset Control SchDoc



CONDITIONS
INITIATION

FPGA EP3K5 [1..256]

SRAM



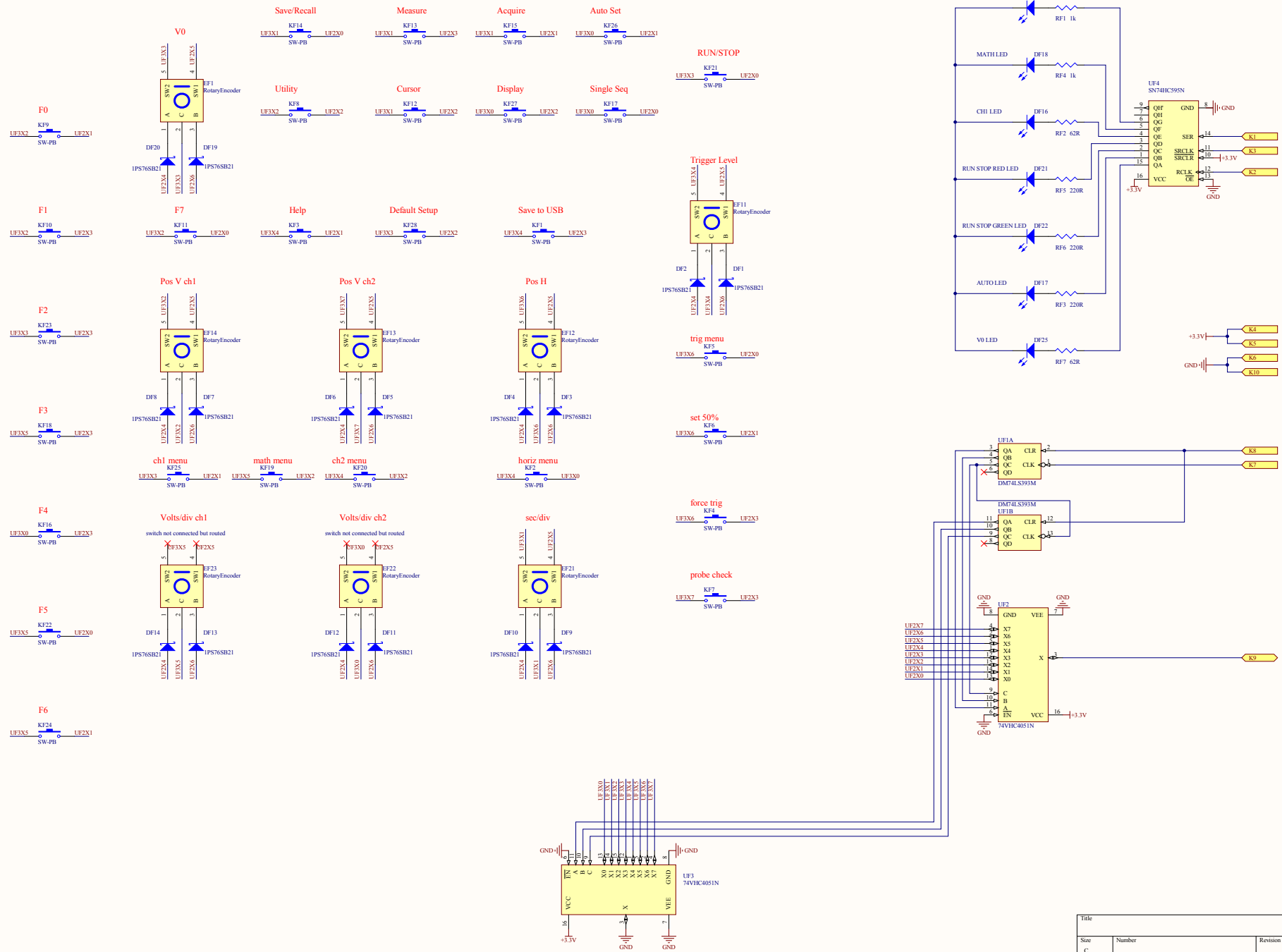
CPLD MAX II [1..100]

CPLD MAX II [1..100]

CPLD MAX II [1..100]

Title		
Size	Number	Revision
C		
Date:	1/25/2011	Sheet of
File:	C:\Development_00\DSO Flow SchDoc	Drawn By:

Front Panel Circuit



Title		
Size	Number	Revision
C		
Date:	1/25/2011	Sheet of
File:	C:\Development_07-FrontPanel\SchExc	Drawn By: