NCP5351

Theory Of Operation

Enable Pin

The Enable Pin (EN) is controlled by a logic level input. With a logic level high on the EN pin, the output states of the drivers are controlled by applying a logic level voltage to the CO pin. With a logic level low both gates are forced low. By bringing both gates low when disabling, the output voltage is prevented from ringing below ground, which could potentially cause damage to the microprocessor or the device being powered.

Undervoltage Lockout

The TG and BG are held low until V_S reaches 4.25 V during startup. The CO pin takes control of the gates' states when the V_S threshold is exceeded. If V_S decreases 300 mV below threshold, the output gate will be forced low and remain low until V_S rises above startup threshold.

Adaptive Nonoverlap

The Adaptive Nonoverlap prevents a condition where the top and bottom MOSFETs conduct at the same time and short the input supply. When the top MOSFET is turning off, the drain (switch node) is sampled and the BG is disabled for a fixed delay time ($tpdh_{BG}$) after the drain drops below 4 V, thus eliminating the possibility of shoot−through. When the bottom MOSFET is turning off, TG is disabled for a fixed delay ($tpdh_{TG}$) after BG drops below 2.0 V. (See Figure 2 for complete timing information).

Layout Guidelines

When designing any switching regulator, the layout is very important for proper operation. The designer should follow some simple layout guidelines when incorporating gate drivers in their designs. Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace. The use of a ground plane is a desirable way to return ground signals. Also, component location will make a difference. The boost and the V_S capacitor are the most critical and should be placed as close as possible to the driver IC pins, as shown in Figure 4(a), C21 and C17.
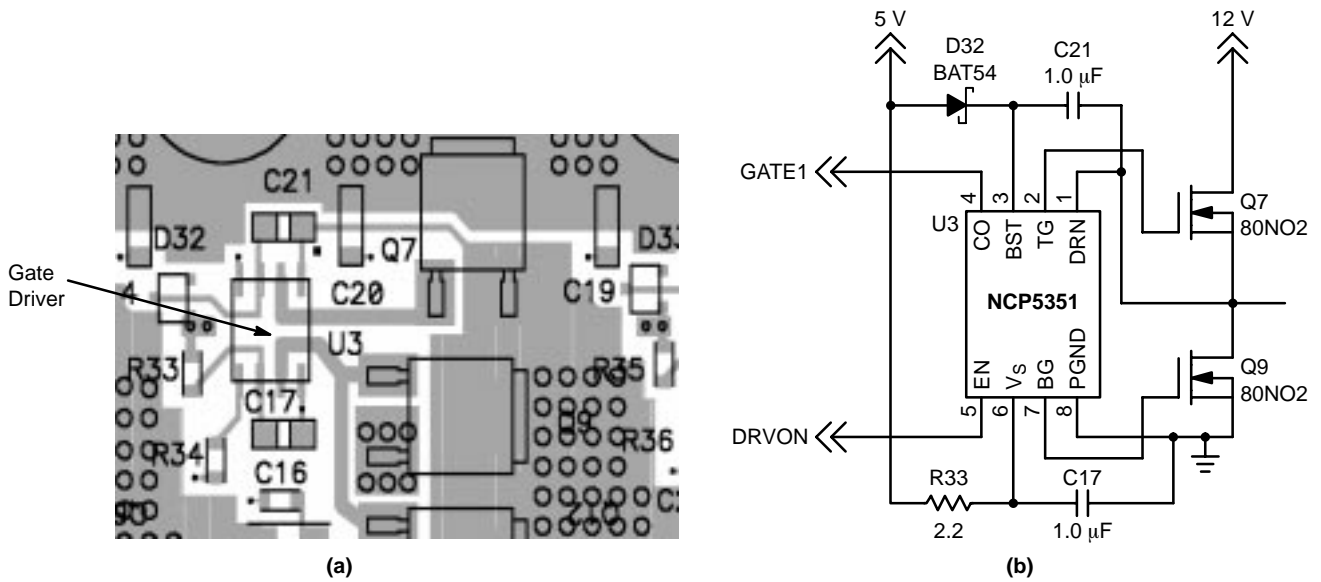

Figure 4. Proper Layout (a), Component Selection (b)