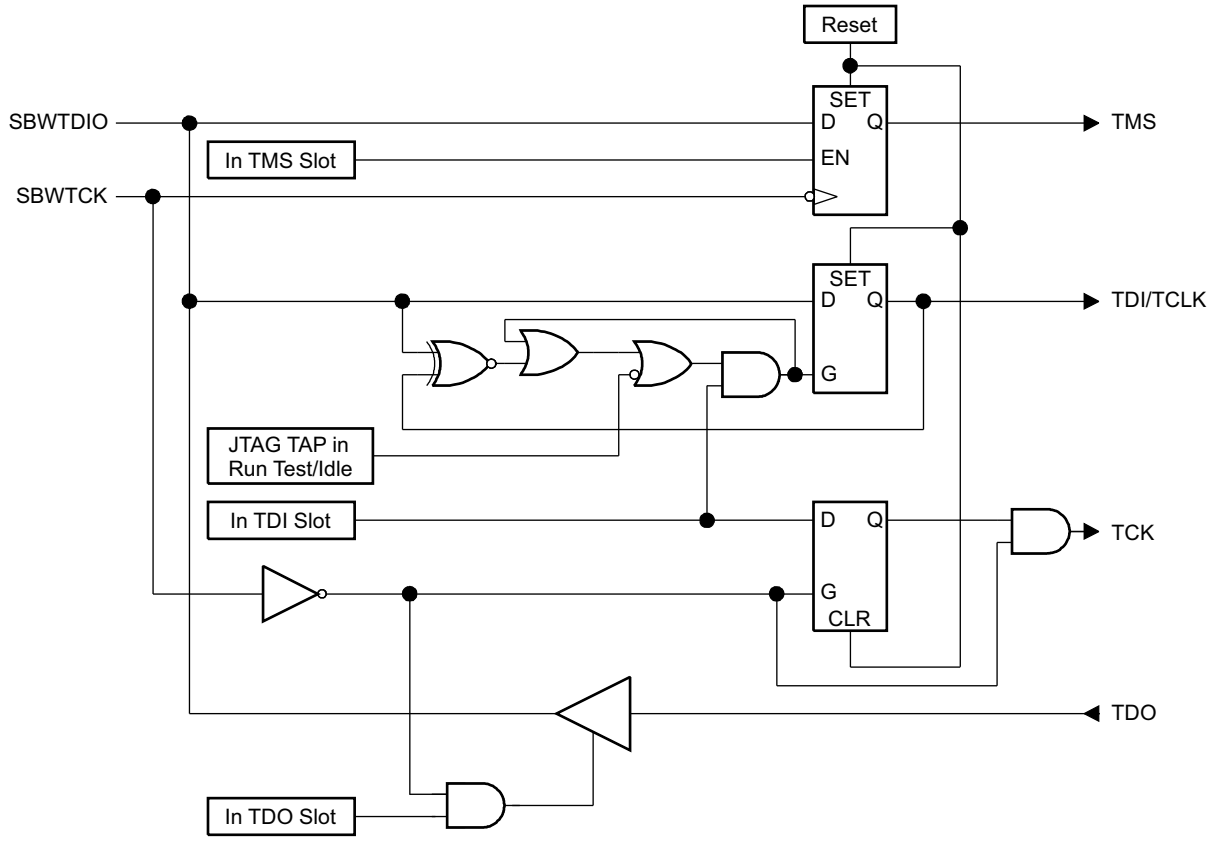

Figure 2-9. SBW-to-JTAG Interface Diagram

The advantages of this implementation are:

- Data on TDI and data on TDO are aligned.
- During the TDI_SLOT of the 2-wire interface, SBWTDIO can be used as TCLK input if the JTAG TAP controller is in its Run-Test/Idle state. For this purpose, the TDI output must be synchronized to its input as shown in Figure 2-11. The synchronization logic is only active in the Run-Test/Idle state.

After power up, as long as the SBW interface is not activated yet, TMS and TDI are set to logic 1 level internally.

2.2.3.2 TMS Slot

The TMS Slot is used to switch between states in the TAP Controller state machine (see Section 2.1.2) of the JTAG module of the target device. The following macros are located in the LowLevelFunc header file in the Replicator example project.

2.2.3.2.1 TMSH Macro

Sets SBWTDIO high for TMS slot (no special TDI preparation handling)

- Set SBWTDIO high
- NOP 5 cycles (delay at 18 MHz)
- Set SBWTCK low
- NOP 5 cycles (delay at 18 MHz)
- Set SBWTCK high

2.2.3.2.2 TMSL Macro

Sets SBWTDIO low for TMS slot (no special TDI preparation handling)

- Set SBWTDIO low
- NOP 5 cycles (delay at 18 MHz)
- Set SBWTCK low
- NOP 5 cycles (delay at 18 MHz)
- Set SBWTCK high