AN76496

PSoC® 5LP – Solar Microinverter Control Design

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To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/an76496.

AN76496 describes a possible approach to a solar microinverter design using PSoC® 5LP. In this application note, you will find some light discussion on what a solar microinverter is and what its defining characteristics are. Most of the discussion centers on how you can use PSoC 5LP to control all aspects of the microinverter.

Note: The power and control hardware described in this application note are not available for sale. Design files for the control card are available in the zip file with this application note.

Contents

Introduction

The sun has been a source of energy and will likely continue to be so for a very long time (probably longer than my colleagues and I will be around). It produces about 384.6×10^{24} Joules of radiated solar energy every second[1]. We can capture at least a tiny percentage of that vast energy and convert it into electrical energy for everyday use.

This application note introduces a DC-to-AC converter design, an inverter (Figure 1). However, this inverter design is specifically targeted at converting highly variable energy from a single solar panel into a form that can be injected directly into the power grid, the same grid that delivers energy to your home. This is often referred to in the solar industry as a grid-tied solar microinverter.

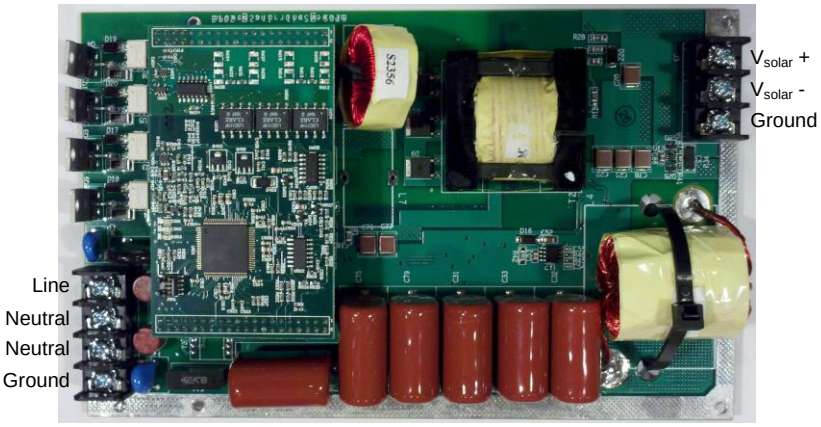
This application note emphasizes the control design and how PSoC 5LP is employed for this particular power topology rather than discussing the power stage design. There are numerous topologies in use today and probably many more yet to be discovered that perform inversion in a cost- and energy-efficient way. PSoC 5LP is well equipped to be the central control for almost any current or inverter design yet to be discovered.

Please note that DC-to-AC converter design is a detailed subject rooted in power electronics. However, the fundamentals of power electronics, and the power stage design, fall outside the scope of this application note, a very interesting and vast subject by its own right. This topic is left for you to explore if you don't already know it.

In addition, this application note assumes that you are familiar with developing applications using PSoC Creator™ for PSoC 5LP. If you are new to PSoC 5LP, you can gain perspective by reading or skimming AN77759, Getting Started with PSoC 5LP. If you are new to PSoC Creator, go to the PSoC Creator home page for an abundance of information about the world's leading development environment for programmable mixed-signal systems.

[1] Information about our sun is available from NASA: http://nssdc.gsfc.nasa.gov/planetary/factsheet/sunfact.html

Figure 1. PSoC 5LP Controlled Microinverter



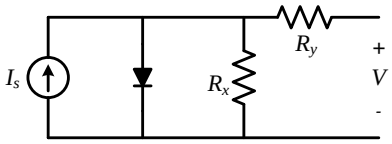
Solar Panels

Although this application note centers on a particular inverter design and how it applies to PSoC, let's start with at least a cursory discussion about photovoltaic cells and panels.

Solar Cell Model

On a basic level, a solar panel looks like a current source driving into a diode and out through some losses. Figure 2 shows the widely known model for a solar cell.

Figure 2. Solar Cell Model



The short circuit current (I_s) minus the diode (I_D) and internal shunt (R_x) current equals the solar cell output current.

Equation 1 $$I = I_S - I_D - \frac{V_D}{R_X}$$

The diode voltage in Figure 2 is, of course, the sum of the voltage drop across the series resistance and the output voltage.

Equation 2 $$V_D = V + IR_y$$

Finally, the classic voltage-current relationship for a diode is shown in Equation 3.

Equation 3 $$I_D = I_0\left(e^{\frac{q}{nkT}V_D} - 1\right)$$

Combining the previous three equations yields a solution for output current. Unfortunately, that solution is not directly solvable without some entertaining numerical analysis.

Equation 4 $$I = \left(I_S - I_0\left(e^{\frac{q}{nkT}(V+IR_y)} - 1\right) - \frac{V}{R_X}\right)\left(\frac{R_X}{R_X+R_y}\right)$$

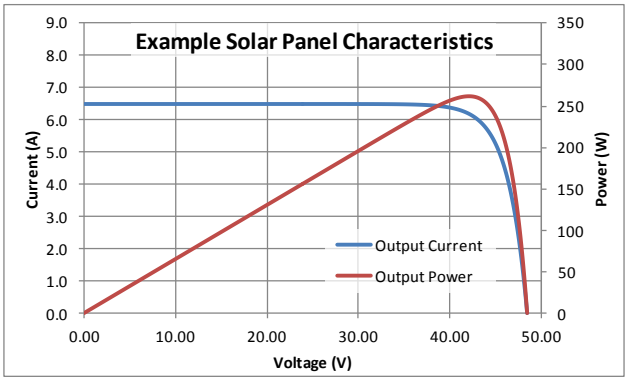
So, what does all this mean? Solar cells are complex devices that have voltage and current characteristics that depend on each other. Therefore, solar cells are not purely voltage sources, nor are they purely current sources. Also, with such voltage and current dependencies, there is clearly a balancing point between the voltage and current where the power output is matched to the internal power loss. The result is a peak output power for a solar cell.

Solar Panels

While Equation 4 shows a relationship for a single cell, a solar panel is a combination of cells. Large arrays of cells combined into a single panel can yield much higher voltage.

Solar panels vary significantly in output capability, but they all bear the same major characteristic that defines a single cell: There is a point at which the solar panel delivers the highest amount of energy. Figure 3 shows an example of the characteristics for a panel that has an open-circuit voltage of about 48 V and a short-circuit current of about 6.2 A. Note that this example is a simple approximation; panel characteristics vary with irradiance and temperature.

Figure 3. Example of a Solar Panel's Characteristics



About Grid-Tied Solar Microinverters

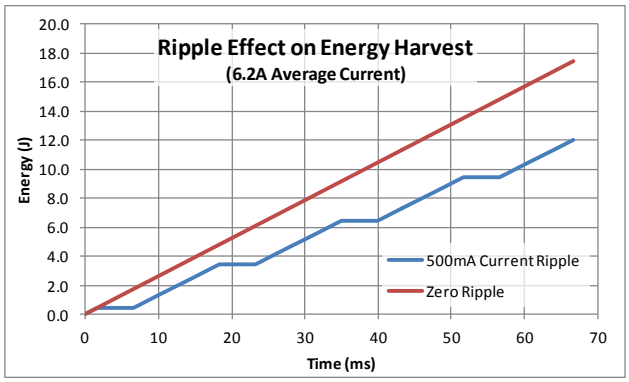
Many characteristics define a grid-tied solar microinverter. Included are control and other functional features designed to allow the maximum energy harvest and safe operation on the AC grid. In the following subsections, we look at the basic features of a grid-tied solar microinverter. If you are familiar with these features and simply want to learn about the PSoC-based implementation, skip these subsections.

Ripple Control

It is possible to pull energy at the peak power point of the solar panel, but the current (and voltage) must be relatively confined to the region where the solar panel delivers the most energy. If the current leans too high or too low, then the voltage on the panel swings based on the reflected characteristics of the panel. As a result, excessive current or voltage ripple could easily push energy harvest off of the ideal target.

Take this situation, for example. A constant current source is pulling 6.2 A from the fictitious solar panel with the characteristics noted in Figure 3. Figure 4 shows the energy harvesting results over four AC line (60-Hz) cycles. In one case, 500 mA of ripple is mixed with the average. In the other case, there is no ripple; it is pure DC current. It is clear that with just 500mA of ripple, the panel voltage is collapsing to the point at which no energy is being pulled for brief periods. Therefore, the energy harvest is much lower for the panel with the extra ripple. Although this solar panel model is fictitious, the situation depicted is real. The ripple on the solar panel must be quite low to maximize the energy harvest.

Figure 4. Ripple Effect on Energy Harvest



Maximum Power Point Tracking

As mentioned, you cannot achieve the peak energy harvest without managing the ripple. Likewise, peak energy harvest is not possible without a control method to find the peak energy output. Keep in mind that because solar panels are located in an open environment, their harvesting capability depends on conditions such as irradiance and temperature. The irradiance and temperature vary enormously as weather patterns change, the earth rotates, and the seasons vary. This control method is generally called Maximum Power Point Tracking (MPPT).

From a 5000-foot view, MPPT is simple: Control the solar panel current consumer to achieve the highest possible energy delivery. The amplitude of the AC current injected into the grid is modulated up or down to a point at which the highest possible energy is harvested from the solar panel. Voltage and current information is taken from the solar panel to determine the power and, therefore, the energy. Use that information, and a history of energy harvest, to determine whether the peak current injected into the grid can increase or decrease to improve energy harvest. Basically, the MPPT control perturbs the system current control and observes how the energy harvest changed.

Long Life

Manufacturers of solar panels typically guarantee them for a long time—a 25-year life is common. A microinverter is often mounted directly to the panel and sold together as a unit. Therefore, it makes sense to match the life of the inverter to the solar panel. A 25-year life is a long time, especially for electronic equipment exposed to the harsh conditions of an outdoor environment.

Because of the long life expectancy and harsh conditions, you need to choose components that are robust and an architecture that favors those components. The most common stress point for any experienced hardware engineer probably is electrolytic capacitors. The inverter topology described in this application note uses an active ripple control method with more robust film capacitors to avoid the sensitivities of using electrolytic capacitors.

Line Synchronization and Monitoring

Line synchronization is integral to the inverter because everything about inversion is managed in sync with the AC line. This is natural because we want to inject energy back into the grid, not take it away. And that is done by keeping the power factor as close to unity as possible. Therefore, tight synchronization to the grid is critical.

In addition to synchronization, the line is monitored for frequency variation and voltage variation, which is closely coupled with active islanding detection methods.

In a design that we describe later, synchronization is used for more than control and monitoring. Many functional aspects of the design rely on synchronization to function.

Anti-Islanding

Anti-islanding is a safety feature of a grid-tied inverter. If the grid were to go down, then there is the risk that an array of inverters harvesting energy from the sun has enough energy delivery capacity to supply the local grid. Therefore, you might say that there is an “island of power” being generated even though the grid is technically off.

This is a safety hazard; there is a reasonable chance that the grid is off for a reason, and energy is not desirable at that moment. Anti-islanding is designed in to detect when the microinverter is no longer connected to an active grid and shuts down in such situations.

Spec Guidance

A microinverter is a grid-connected system, which is required to adhere to standards that ensure the safety and integrity of the system. Here are a couple of the more obvious standards, depending on the geographical region:

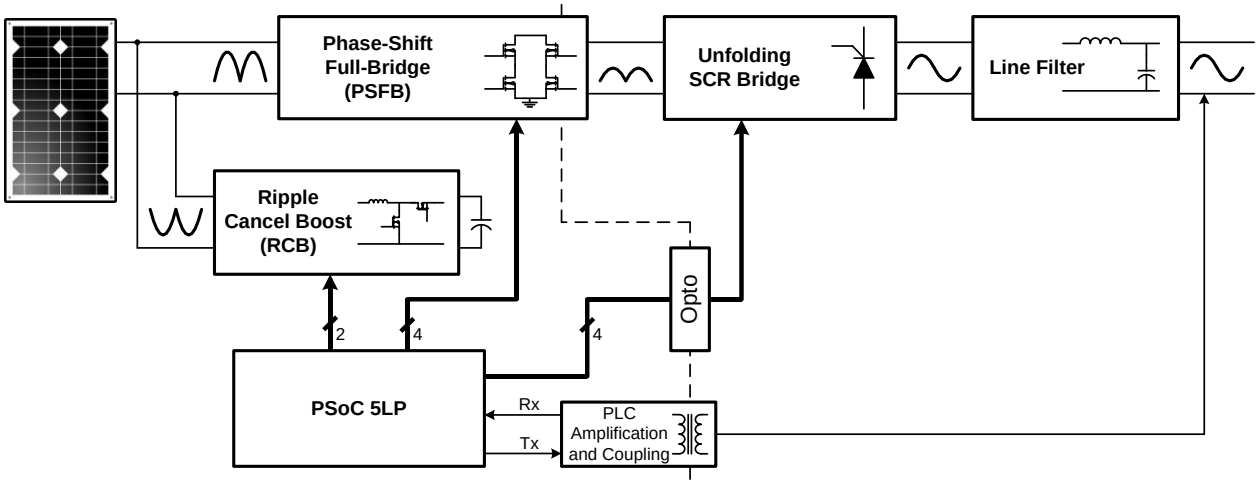
- IEC EN 61000 – Electromagnetic Compatibility
- IEEE1547 –Interconnecting Distributed Resources with Electric Power Systems
- UL 1741 – The Use of Inverters, Converters and Controllers In Independent Power Production Systems
- VDE 0126-1-1 – Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid

The Microinverter Power Topology

To better understand the control algorithms, which will be discussed later in more detail, you need to gain a sense of the topology for this inverter. Figure 5 shows a basic block diagram of the inverter. There are three stages that shape the voltage and current signals and, eventually, transfer energy:

- Phase-Shift Full-Bridge (PSFB) – It is modulated at high frequency, about 100 kHz, to generate a rectified sine wave. The rectified sine wave is the exact size and shape of the grid voltage except that it is a rectified reflection of the grid. Likewise, the current from the panel is shaped to follow the grid voltage.
- Silicon Controlled Rectifier Bridge (SCRB) – This is basically the same as a bridge rectifier found in almost any power supply; however, each diode in the bridge is a thyristor, which is controllable. The unfolding SCRB operates at the rate of the grid, and it unfolds the rectified current onto the AC grid.
- Ripple Cancel Boost (RCB) – Note that there is a boost converter hanging off the connection between the solar panel and the PSFB. This is a synchronous boost converter that pulls energy from the solar panel when the PSFB is not pulling energy. When the PSFB is pulling high energy, the boost converter changes direction and transfers energy in the reverse direction. The net effect is that the ripple reflected on the solar panel is canceled. This is also known as an active filter.

Figure 5. Inverter Architectural Overview



The Microinverter Control Architecture

Because the microinverter power conversion topology contains three major conversion stages, there are at least as many control stages that directly control or interact with the conversion stages. In fact, many functional elements make up the control of the microinverter. They will be discussed in some detail in the following sections. Here is a brief summary of some of the key control functions:

- Ripple Cancel Boost Control – This is a control algorithm that drives the synchronous boost converter to keep the ripple off the solar panel.
- Output Current Control – This specifically applies to the control algorithm commanding the PSFB to force the output current of the microinverter to follow a sinusoidal shape. Also note that this is probably the most complex of all the major control pieces in this design.
- Phase Locked Loop – The PLL synchronizes the internal controls to the grid, and it, too, is a basic control loop.
- Maximum Power Point Tracking – The MPPT is a complex control for quickly finding and holding the peak power in the system. In many ways, it is more of an algorithm than it is a control.

Figure 6 shows a larger view of the DC/AC control. Many of the more complex details are hidden as functional blocks, which will be presented in more detail.

Figure 7 presents the larger picture of the boost control. Again, many of the finer details are abstracted into functional blocks that will be explained.

Figure 6. Microinverter Control Architecture Part 1 – DC/AC Control

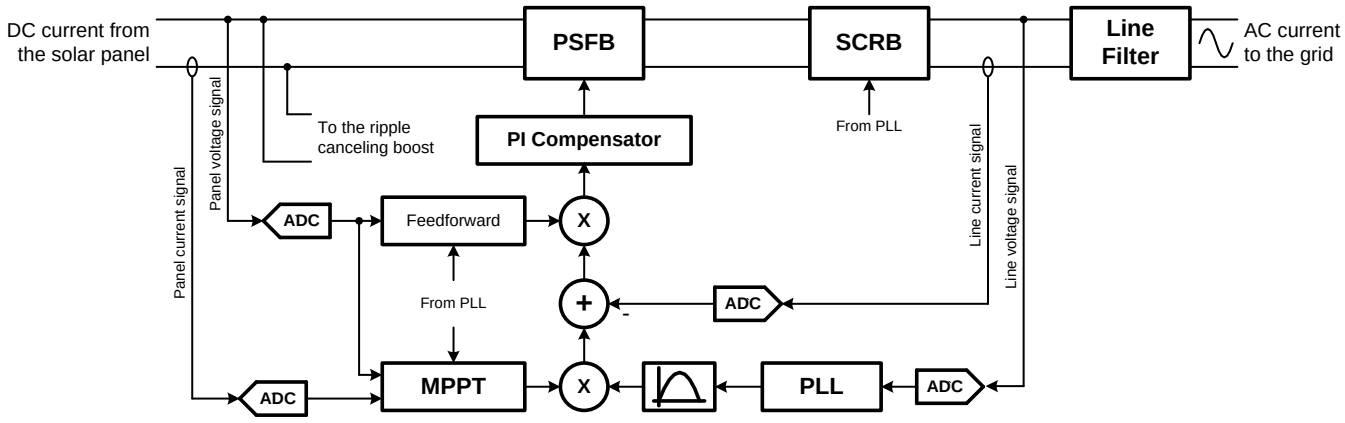
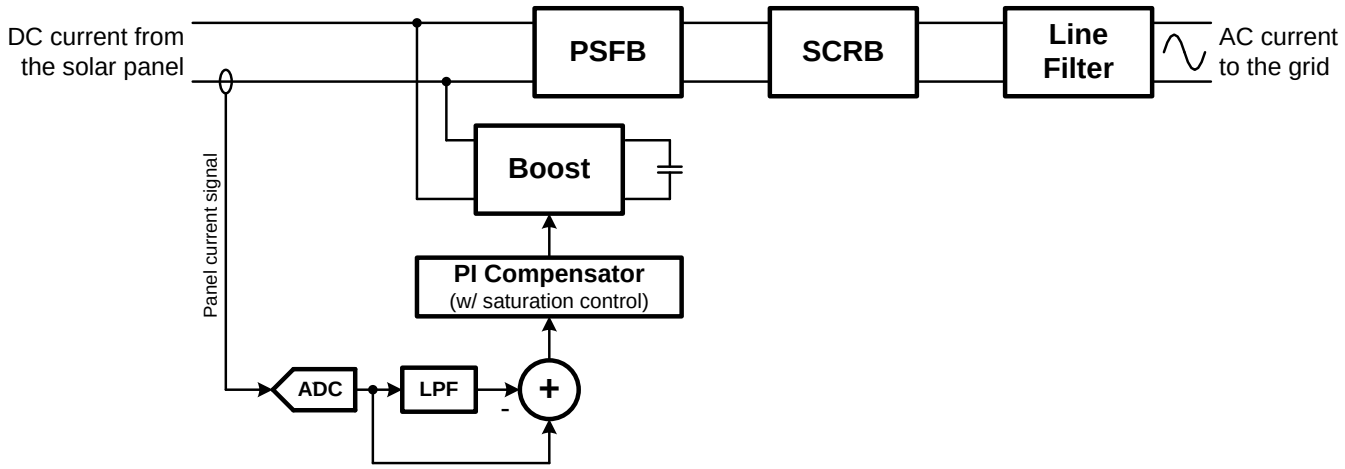


Figure 7. Microinverter Control Architecture Part 2 – Ripple Control



DC/AC Control

The DC/AC control is exactly as the name implies. The converter stages combined with the modulation schemes and control algorithms transform the DC input from the solar panel to a fully sinusoidal signal driven to the grid.

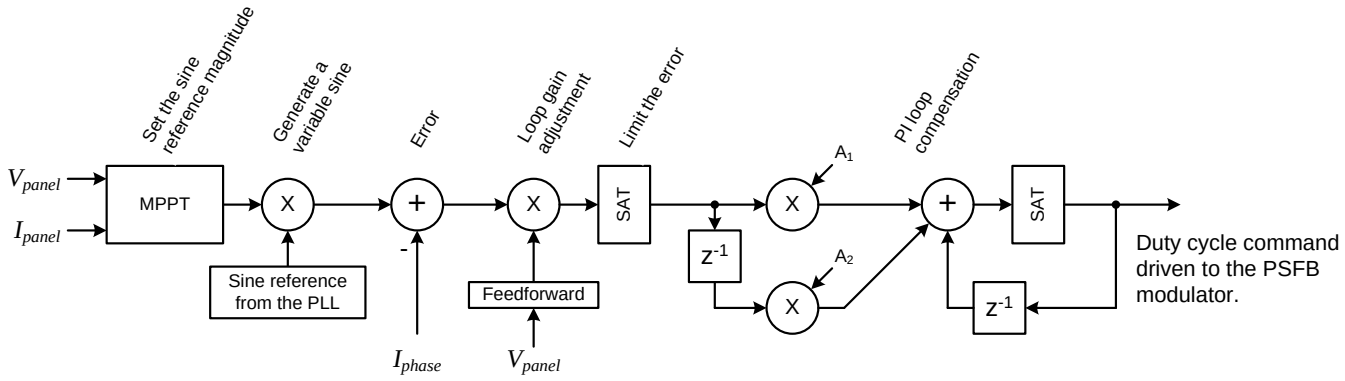
The Control Algorithm

The goal of the inversion control is to re-create a sinusoidal wave or, in this case, a half wave of current to be injected into the AC grid. The PLL is responsible for creating the reference wave; however, the wave is of a fixed magnitude and represents only the desired shape. Therefore, the half sine reference from the PLL needs to be scaled appropriately, and the MPPT algorithm is responsible for providing that. The MPPT algorithm generates a scaling reference, which is mixed with the half sine. The result is a moving reference that is a half sine in shape and has a magnitude that varies based on the desired average energy targeted to be pulled from the solar panel.

The varying sine reference signal is compared with the sensed grid current (I_{phase}) to generate an error signal. The error signal is fed into the controller.

The controller is composed of two parts. The first is a gain stage in which the error signal magnitude is scaled according to the solar panel voltage. This is important to maintain good control over a wide operating region, because the loop gain is sensitive to input voltage variation. The output of the feed-forward is saturated to limit the signal into the next part of the controller, which is simply a generic form of proportional-integral compensation. Figure 8 shows the complete control design for the DC/AC control.

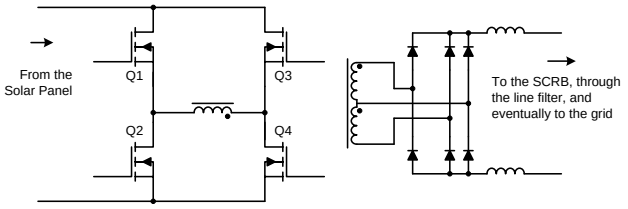
Figure 8. Phase-Shift Full-Bridge Control Algorithm



Control Background Information

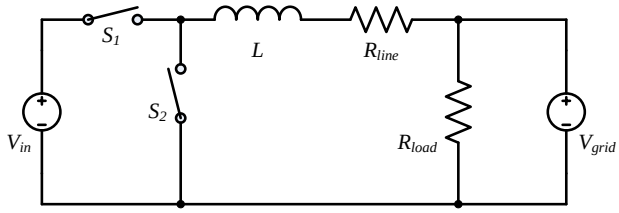
To appreciate the control design, it is important to get some perspective on the converter being controlled. The full-bridge shown in Figure 9, which more accurately represents the bridge in the inverter, is generally considered among the class of forward converters, which, as forward converters go, are “buck” derived.

Figure 9. Basic Full-Bridge



Given that the phase-shift modulated full-bridge is a “buck” derived converter, we model it as a buck to expose some of the basic features, albeit the transformer, of course, represents gain that we grossly ignore. Figure 10 shows the extremely simplified model in the form of a classical buck converter driving a resistive load and connected to a source at its output (this is a fictitious grid). Included is some series loss, representing the line impedance and the variety of other losses in the path to the actual load. Note that there is no output capacitance either, which is not strictly true. There is capacitance; however, it is quite small and adds little to this basic discussion. As you can see, this is very different from an exact representation; however, it captures the essence behind the control design.

Figure 10. Basic Model



Equation 5 $$\frac{\hat{\imath}_L}{\hat{d}} = \frac{V_{grid}}{R_{line}} \frac{1}{\left(s\frac{L}{R_{line}}+1\right)}$$

The small-signal response (see Equation 5) is easily derived from the circuit model shown in Figure 10. Clearly, the system is dominated by a single pole. That suggests that all that is needed to build a stable design that regulates well is a PI compensator. The second major feature that is exposed is that the gain is proportional to the input voltage. This is critical to know because the voltages from the panel probably are not consistent. As a result, feedforward is employed to adjust the loop gain based on input voltage. The third major feature is that the series losses have an impact on this design; therefore, the losses that are knowable are accounted for with additional margin for what is not known.

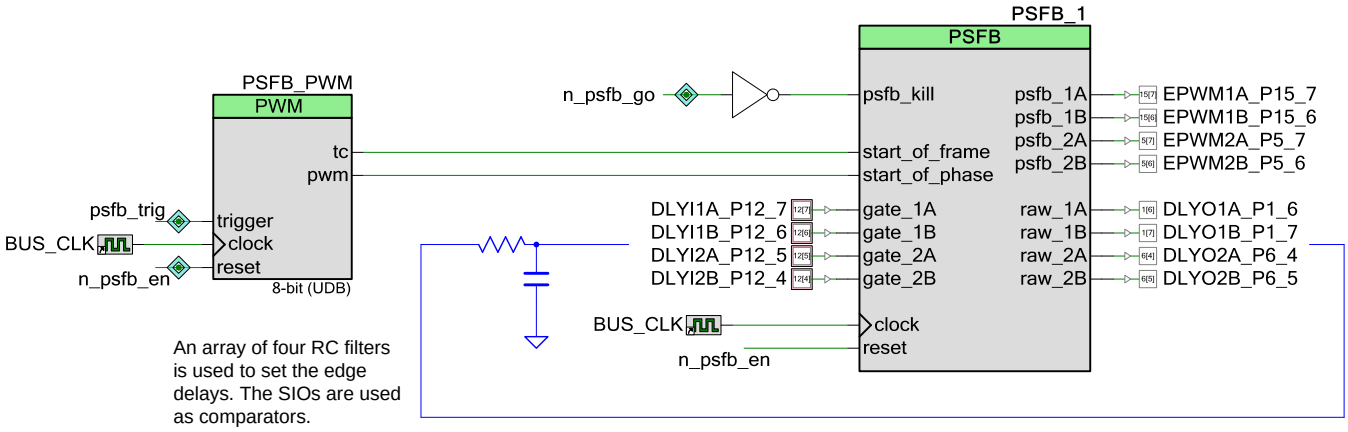
Phase-Shift Full-Bridge Modulation

The PSFB modulation is interesting enough that it was made it into a Creator component, and it is described in AN76439.

Figure 11 shows the modulator design captured within Creator. An external modulation (a standard UDB-based PWM component) is used to provide base modulation that is externally synchronized from a master. Therefore, all switching edges that are derived from the same master are deterministic relative to each other, and the PSFB is no exception.

As expected, individual edge delay is necessary to prevent shoot-through in the full-bridge. It is employed by using generic output pins driving into SIO pins through RC filters. The SIO pins are configured as comparators with their reference set at 50% of V_{DDIO}. Thus the time constant of the filters sets the delays. Each phase of the PSFB has its own rising edge delay control.

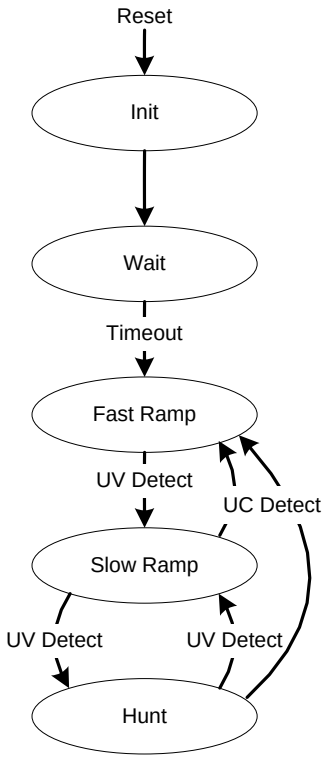
Figure 11. Phase-Shift Full-Bridge Modulation from PSoC



Maximum Power Point Tracking

MPPT is a relatively complex algorithm used to efficiently find the point at which the solar panel delivers the most energy.

Figure 12. MPPT Operating States



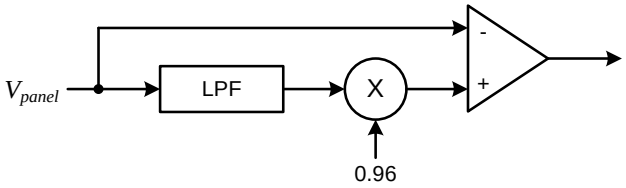
The algorithm employed operates from one of five states. Figure 12 presents that larger picture of the state machine for peak power tracking. Let's summarize:

- Init – This is a temporary state in which the algorithm is completely reset for peak tracking.
- Wait – There are some digital filters that are not likely to be settled, including average power and voltage. This is a built-in delay to allow filter settling before actively searching for the peak power point.
- Fast Ramp – During the fast ramp, large current steps are driven to the DC/AC control to quickly scan for the gross peak.
- Slow Ramp – This is functionally the same as the fast ramp; however, the step size is significantly lower. The result is a narrower find of the peak.
- Hunt – This is the final state. The process, through deep integration, builds a lot of information about the peak power out of the panel and refines the search for the peak.

Fast and Slow Ramp

The fast and slow ramp states are functionally the same with one minor difference that we have not yet discussed. The peak output of a panel has a major defining characteristic. If you slowly, but consistently, sweep up the current, the voltage will gradually fall based on the series losses in the panel until the knee of the power curve is hit. At that point, the voltage drop is significant and measurable. Therefore, one approach to find the peak is to sweep the current until a change in voltage is significant, at least significant relative to the desired operating point. Figure 13 shows a relatively simple-to-code differential detection algorithm.

Figure 13. MPPT Voltage Change Detection



Although the peak detection algorithm is quick to find the approximate peak, it is gross in its targeting. It will only put the control in the approximate range of the peak. The method in Figure 13 is as time-based as it is level-based because of the filter. It will improve in accuracy if the ramp is slower. Thus there are two states employed. The first is a very fast find while the second is a much slower find.

The fast and slow ramp states transition to the next state by looking for a gross sudden transition in solar panel voltage. When the sudden change is detected, the injected current into the grid is assumed to be too much, and it is pulled back by a small percentage before moving to the next state.

Peak Power Point Hunt

The final state is quite slow. And it must be by nature, because there must be enough integrated power information to know that a change in power really happened. When the DC/AC stage is taking energy from the panel near the peak, changes in the measurable power can be extremely small. Therefore, time is needed to integrate to make an accurate decision.

Figure 14 outlines the algorithm that controls hunting for the peak. The power is computed and deeply filtered to attenuate and average the power from the solar panel.

The fundamental functionality of MPPT is to track differential change in power and adjust accordingly. Thus, after the power computation is the derivative. The difference is used as an indicator of which direction to move. The difference between this power reading and last power reading is near, greater than, or less than zero. The controller adjusts up or down based on the difference.

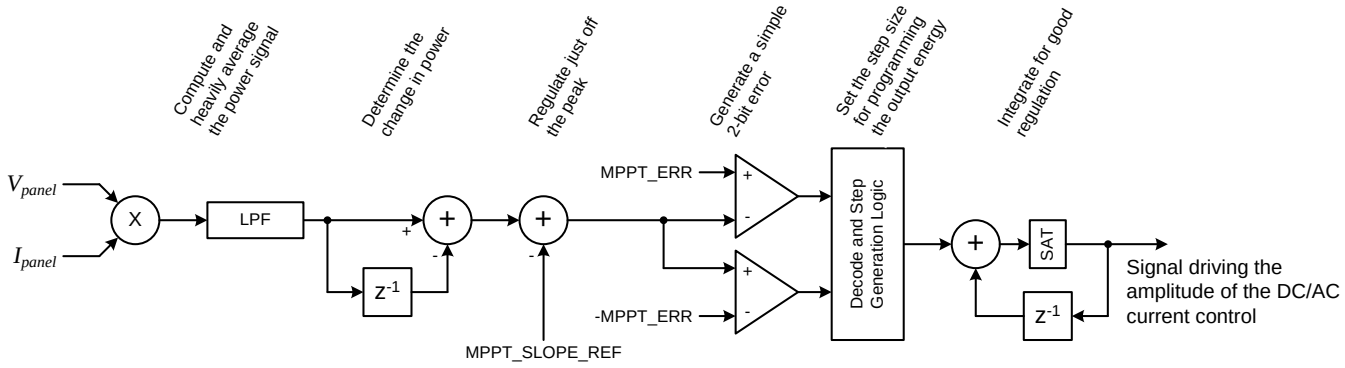
Another basic operation of peak power tracking is to find and track the point at which power is at its peak. Thus, the signal is not monotonic by nature and, therefore, you

cannot control it by normal means. The synchronous direction control latch is specifically designed to address this issue. The direction latch determines the direction the power is trending to select an appropriate gain. When there is a negative power trend, it is assumed the selected direction is incorrect (i.e., chose to go down in current instead of up, and vice versa).

Pure integral compensation provides for good regulation. Because the front-end saturation prevents zero error, the integral compensator ensures that the system is never stable and always hunts for an ideal operating point.

The back-end saturation simply limits the peak power control range. The assumption is that anything out of this range is not defined; therefore, management processes would ideally terminate operation.

Figure 14. Hunt (Perturb and Observe) Algorithm



SCR Bridge Modulation

As Figure 15 shows, the SCRB is the circuit to unfold the rectified current from the PSFB to the grid. The unfolding bridge is implemented using four Silicon Controlled Rectifiers (SCRs) switching at the grid frequency. The devices are placed in an H-bridge configuration. As a result, only a pair of devices is triggered at any given time, depending on the phase of the AC voltage waveform. The PLL is responsible for providing signaling on when to fire and which pair of SCRs to fire.

Figure 15. SCR Bridge Circuit

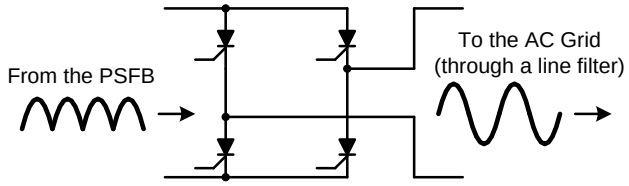


Figure 18 shows the Creator hardware that is employed to trigger the SCRs. Figure 16 and Figure 17 demonstrate the unfolding of the rectified AC into an AC signal, which is injected into the grid after passing through a line filter.

Figure 16. SCR Bridge Positive Phase

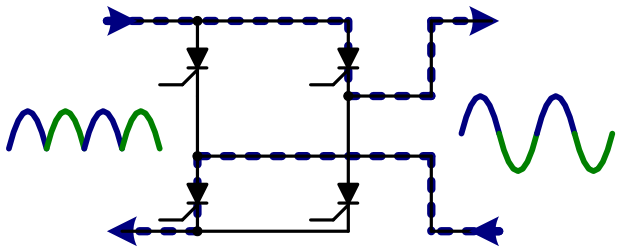
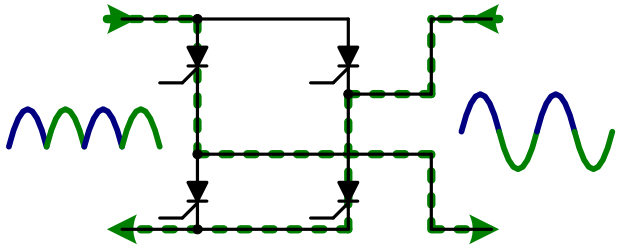
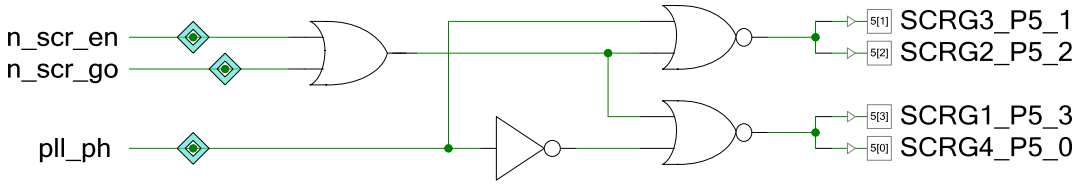


Figure 17. SCR Bridge Negative Phase



Note that SCRs by design need to be triggered with only a small pulse to conduct. An SCR starts conduction provided the applied voltage on the device is forward biasing the device and there is a trigger signal available at the gate terminal of the SCR. The device continues to conduct current as long as the current is above the minimum holding current for the device. After they are triggered, SCRs conduct until the current through them passes below the sustaining current threshold for the device.

Figure 18. Phase-Shift Full-Bridge Modulation from PSoC



Results

Figure 19 shows a scope capture of the output current control in operation. Figure 20 shows the results of the peak power tracking algorithm in action with a snapshot of a solar simulator driving out just under 200 W.

Figure 19. DC/AC Stage Controlled Output Current

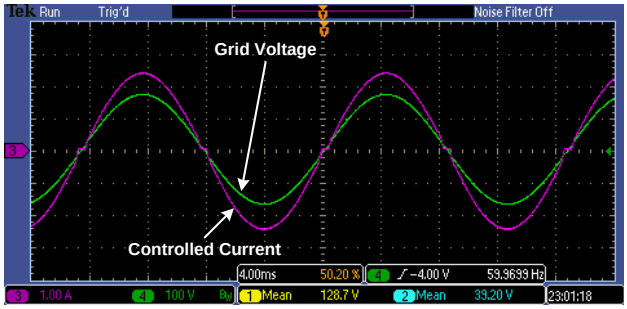
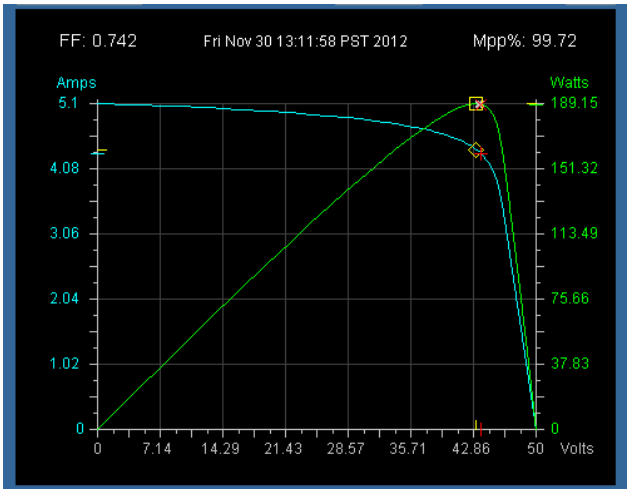


Figure 20. Maximum Power Point Tracking



Ripple Control

The idea behind the boost converter and control is to transfer energy opposite to the current flow into the DC/AC stage. The DC/AC stage is the system moving current into the AC grid. Therefore, you can think of the ripple control as the controller of an energy tank, storing energy when the AC grid does not need it (near the AC grid zero voltage crossing) and releasing that stored energy when the AC grid needs the energy the most (at the peak of the AC grid). Thus, the sum of the current, current to the tank plus the current to the DC/AC stage, results in a DC current (no ripple) being pulled from the solar panel.

The Control Algorithm

To control ripple, you need only compare a relatively wide-bandwidth current signal with a low-bandwidth (heavily filtered) version of itself. The low-bandwidth current signal is the relatively fixed reference for the controller. The high-bandwidth signal is the signal to be controlled. The idea is that the controller programs the duty cycle of the boost to move current as close to the reference signal as possible. Because the average/filtered current is the reference, you could say that the control minimizes the harmonics above the filter cutoff.

The lower half of Figure 22 shows the boost current control. A simple proportional-integral control is employed to take the difference between the high-bandwidth and low-bandwidth current signals and to program the duty cycle of the boost modulator.

The last major piece of this is what to do about the boost output voltage. The boost is connected to an array of film capacitors—the energy tank. Because the control strategy (reference and signal) is entirely based on solar panel current, not boost voltage, there is no control over the boost voltage. Theoretically, the boost output voltage could be anything and control of the current would still be good. But we do not want the boost voltage to “run away” to the point of electrical failure.

Fortunately, the boost is synchronously modulated; therefore, the output voltage is completely driven by duty cycle and does not depend on the conditions on the output of the boost. You simply need to manage the duty cycle out of the controller.

The basic idea is that a saturation window is controlled by a target operating duty cycle. Ripple is allowed to aggressively push on the upper and lower boundaries of

the saturation window, while the window is constantly trying to collapse slowly. The net result is a balance between the ripple controller's need to widen the saturation window and the output voltage controllers' drive to force a steady output voltage. The weight of the two efforts is given to the ripple control to minimize the input current ripple. Therefore, the result is a ripple control that tends to always stay at a target boost duty cycle. That results in constant average boost voltage because it is synchronously modulated on average with the ripple around that. Following that idea, Figure 21 shows a sketch of the boost output voltage.

The top half of Figure 22 shows the boost voltage control algorithm, and it definitely needs a little description. The ripple current control passes up a signal indicating whether saturation has or has not been touched in either direction. Such a saturation event causes the integrator to increase by a static gain; likewise, the lack of saturation causes the integrator to decrease by an alternate static gain. The output stage adds and subtracts this aperture width to/from a duty cycle target. A simple integrator is employed to hold the aperture width. The net effect is that the saturation control block takes a saturation event signal and determines if it needs to aggressively widen or passively shrink the ripple controller's saturation window around a center target. You might think of this as an aperture that is opened or closed around a specific point.

Figure 21. Boost Output Voltage Control

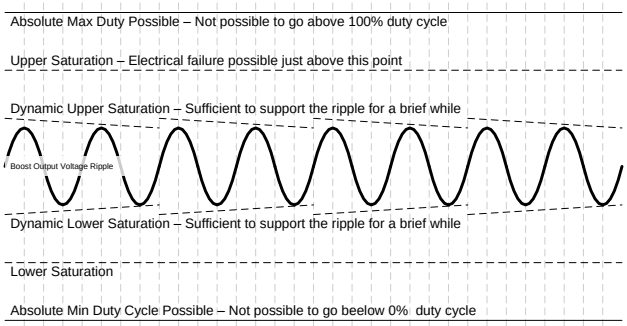
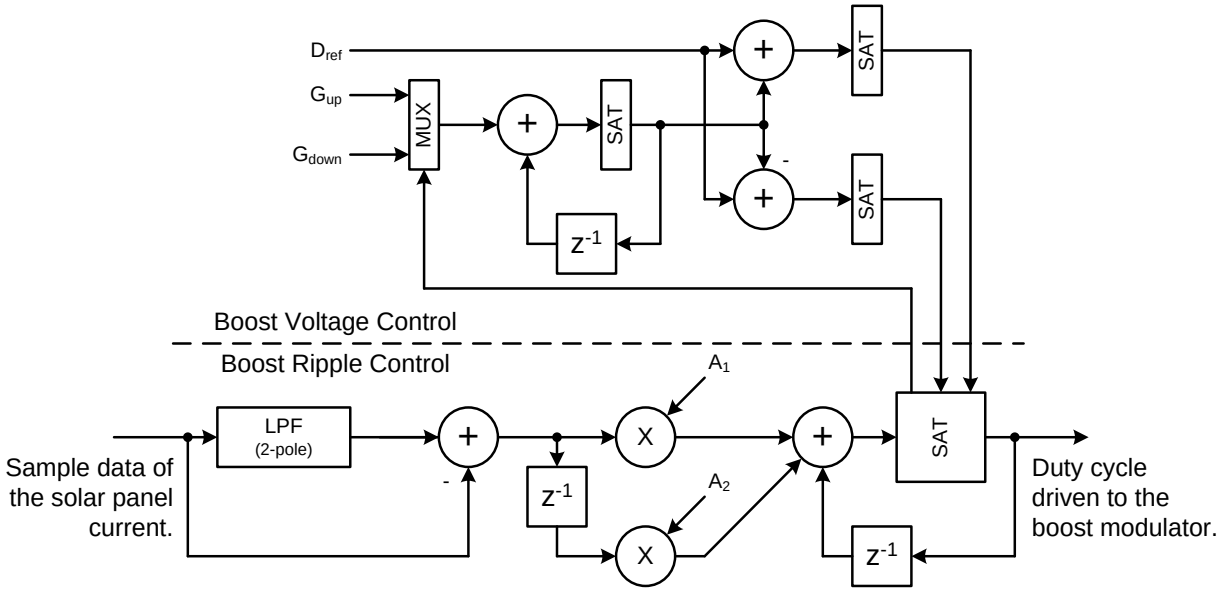


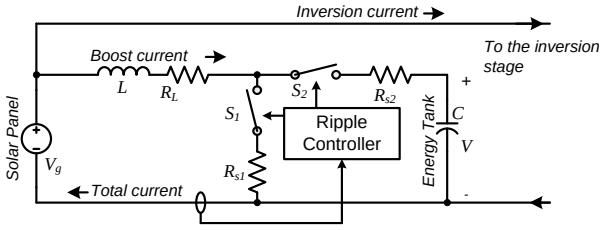
Figure 22. The Complete Boost Control Algorithm



Control Background Information

In this design, the boost converter input current is controlled. Figure 23 presents a basic picture of the boost converter with an abstraction of its control. Through average switch modeling, the small-signal model for the duty cycle to input current is derived in this case, as Equation 6 shows. Although the equation represents a design that is more ideal, it does expose the basic characteristics.

Figure 23. Ripple Control



Equation 6

$$\frac{\hat{\imath}_g}{\hat{d}} = \frac{V_g C}{(D')^2} \frac{s}{s^2 \frac{LC}{DD'} + s\left(\frac{R_L C}{DD'} + \frac{R_{S1} C}{D'} + \frac{R_{S2} C}{D}\right) + 1}$$

Figure 24 shows an example plot of the boost response described by Equation 6. The 90 degrees of phase shift at high frequency suggests a simple proportional-integral control strategy is viable for stable operation.

Figure 24. Boost Input Current Control Response

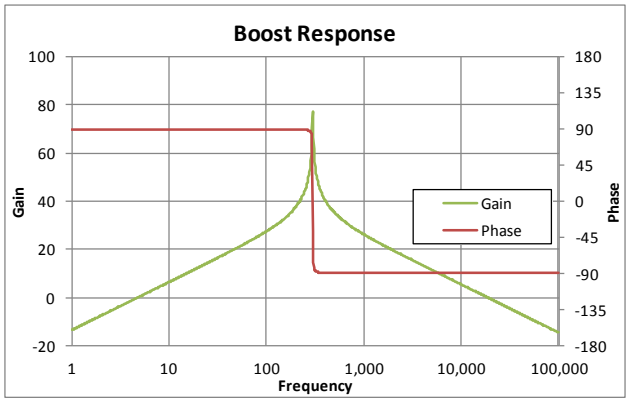


Figure 25 shows an example loop response (the boost response combined with a PI control). You may notice that the low frequency zero in the boost response does not help the performance; the loop response gain is flat over a large region, making it almost synonymous with a proportional controller on a first-order system. However, this is only a model, and a simplified model at that; perfectly flat gain all the way to 0 Hz is unrealistic. Regardless, the approach is sufficient to reduce the ripple.

Figure 25. Boost plus Compensator Loop Response

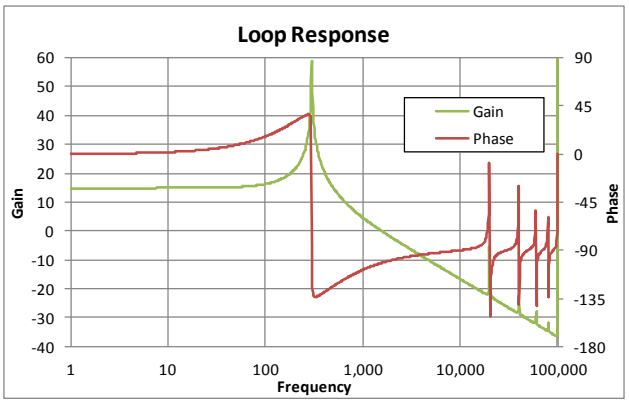
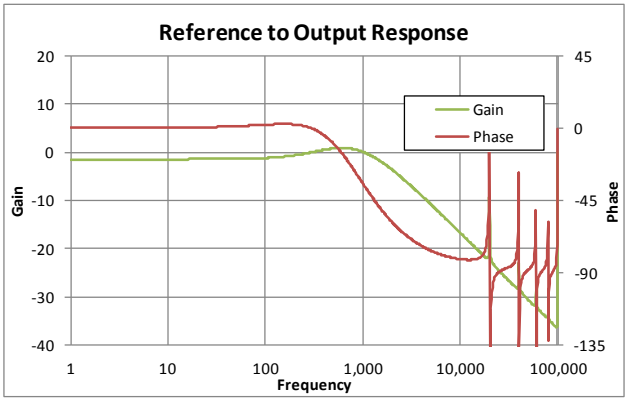


Figure 26 shows an example reference to output response. It is clear by inspecting the distance between the 0db line and the gain response plot that the output will not perfectly follow the reference. This is particularly important around 2x the AC grid rate because this will be the dominant harmonic reflected from the DC/AC control. This relatively moderate control response is because the boost transfer function does not favor great response with a simple PI control strategy.

Figure 26. Boost Input Current Control Response



Boost Modulation from PSoC

The boost modulation is straightforward. A standard Creator PWM component is used with Dead Band enabled. The start of each frame for modulation is a synchronized signal from a master synchronizing source so that all switching edges are in known positions. In addition, some external gating logic is added for quick termination of both phases; both phases are driven low in this situation. Figure 28 shows the Creator schematic and Figure 27 shows the settings.

Figure 27. Boost PWM Setup

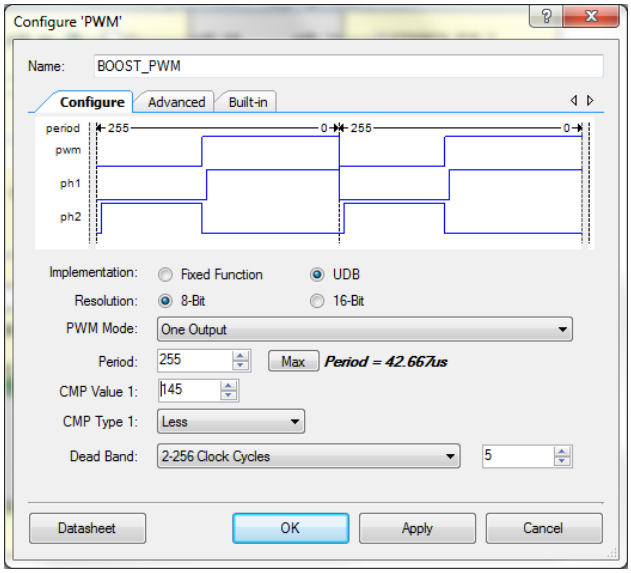
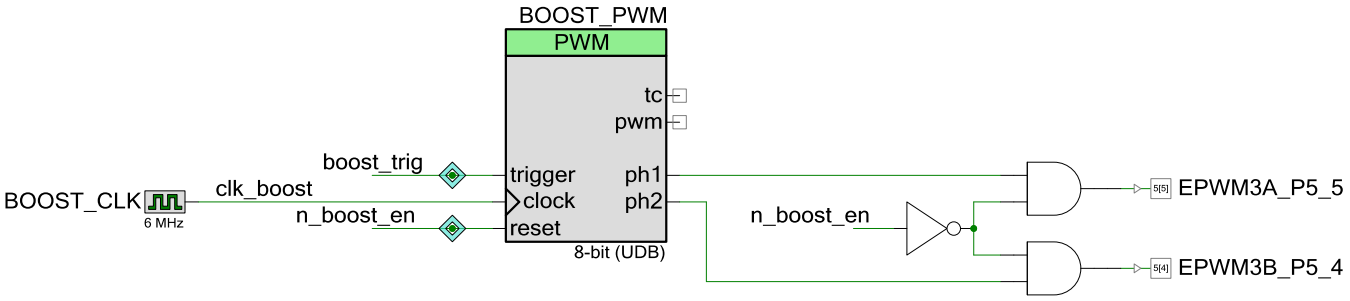


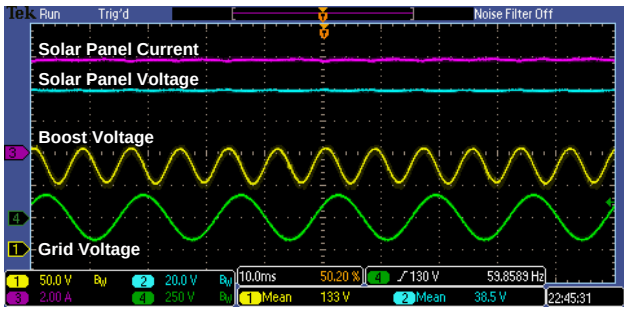
Figure 28. Boost Modulation from PSoC



Results

Figure 29 shows a screen capture of the results. The voltage and current ripple on the solar panel is small but apparent. Notice that the boost voltage contains ripple that would have existed on the solar panel (but not quite the same shape or size) had there not been an active ripple control.

Figure 29. Ripple Control Results



Additional Control Functions

The following subsections describe some of the peripheral features used in the inverter control design.

Event Generation and Synchronization

In the inverter control design, the exact edge placement for a sample is important. For example, in switching power converter designs, the position at which data is taken is critical. Data that is taken exactly on or just after a switching edge in a high power system can be corrupted by the huge amount of noise created. This is due to the large currents and/or voltages that are switched, combined with the hard-to-predict parasitic elements of the system. Therefore, it is advantageous to synchronize data gathering during the “quite” periods of the power conversion, away from the switching edges. Figure 30 shows the synchronizer in which a PWM is used to determine the rate and trigger position of the ADC. In addition, trigger signals shifted in phase are also generated for the boost modulator and the PSFB modulator. Therefore, sampling is positioned where the power converter switching activity has long passed.

Figure 30. Synchronization Logic

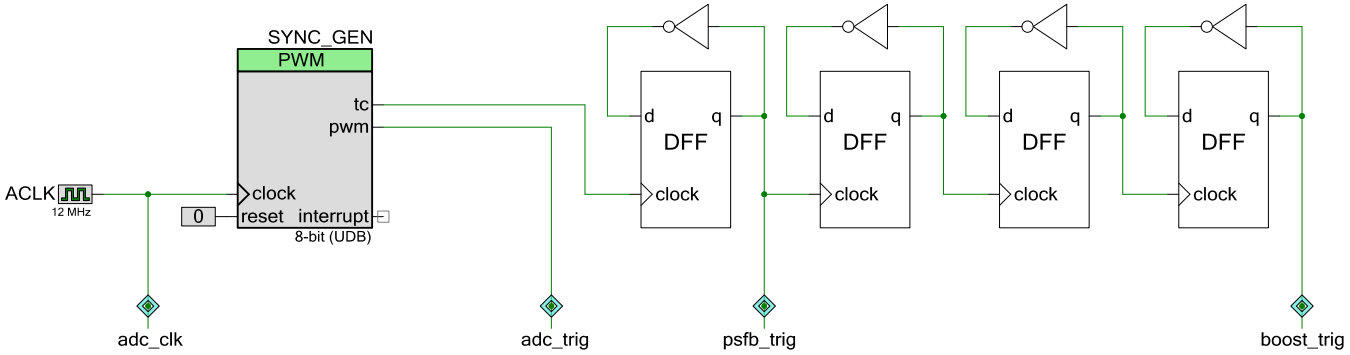
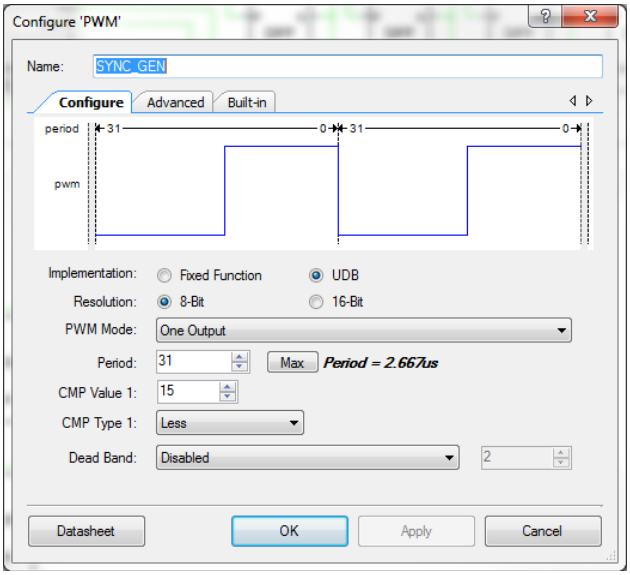


Figure 31. Basic Full-Bridge



Data Gathering and Scheduling

You may have noticed in Figure 6 and Figure 7 that we used multiple ADCs to represent sampling. The reality is that only one ADC is used. Consider the following scenario: You would like to run through a set of analog channels collecting data with one ADC. You want the data to be collected at points in time synchronized to a periodic signal. Most important, because not all channels of data are equally important, they need some scheduling. PSoC can be configured to provide this level of capability with little to no processor overhead.

DMA is an exceptionally powerful tool to be able to offload work from the core processor. To use DMA effectively and efficiently, you need to organize memory in a way that is friendly to DMA (and friendly to the mental fortitude of the designer). In this case, it is advantageous to configure the analog such that analog channels can be selected with a single atomic write operation via DMA. Thus, with a single transaction from DMA, you can select an analog channel for data sampling while all others are unselected. This means that the hardware design and pin selection is given careful consideration; the pins were not arbitrarily chosen.

Figure 32 shows a real example with the analog channels carefully selected to land on pins that align mutually exclusive on the left analog global bus. Thus, the array of switches in the ANAIF_RT_SAR0_SW0 register is treated as a multiplexor.

Scheduling the data to gather is a simple matter of setting a table in memory that represents the channels in order of the schedule. And the table is populated in priority order with time invariance (or time variance if one so chooses). Then DMA is used to sequence through the channels; eight channels are scheduled with the following priority:

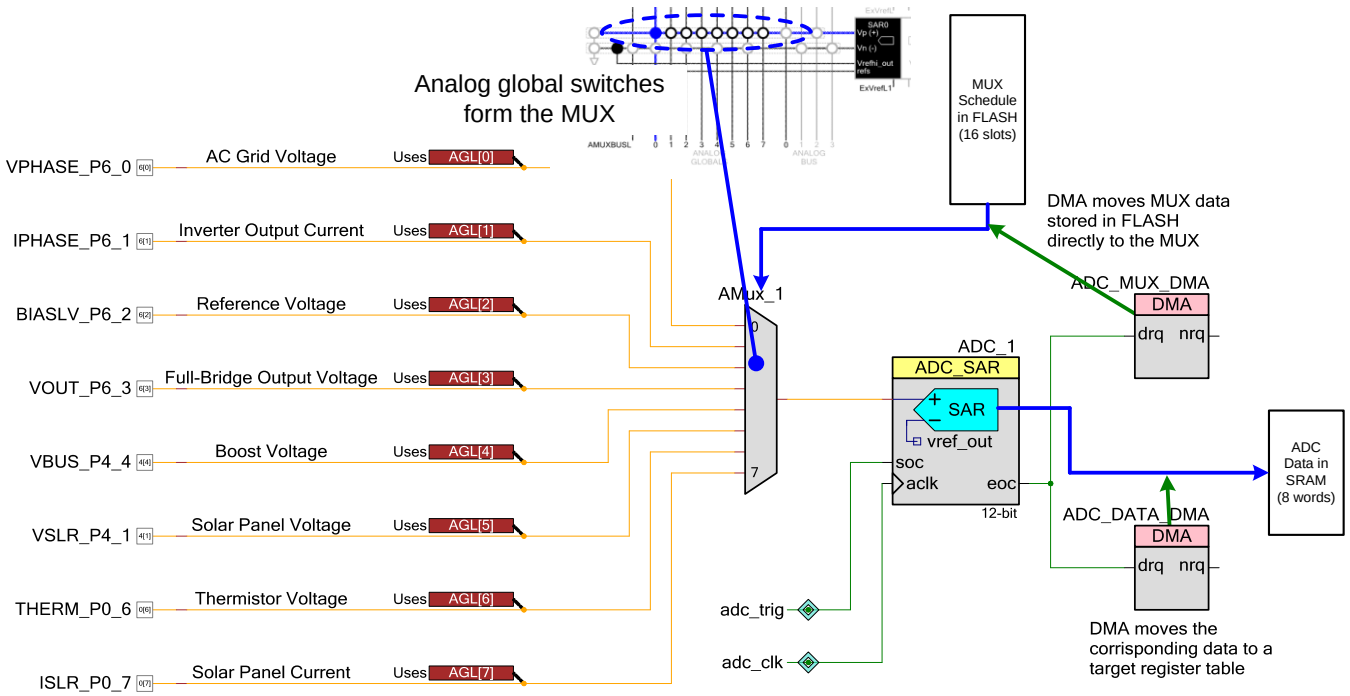
Table 1. Character Set Quick Reference

Analog Channel	Priority	Notes
CH_IPHASE	25%	Half the total schedule is allocated to these two channels, the most important data in the system. In fact the major (and fastest) control operations for this design are derived from these two converted signals.
CH_VPHASE	25%	
CH_ISLR	12.5%	One quarter of the schedule is allocated to these two channels. The data is important, but not as much as the previous two.
CH_VSLR	12.5%	
CH_VOUT	6.25%	The leftover bandwidth is distributed amongst the following data consumers. The data is needed, but it is not needed at a high rate.
CH_BIASLV	6.25%	
CH_VBUS	6.25%	
CH_THERM	6.25%	

DMA is configured to naturally sequence through the table and move the data from flash memory to the switch array. Thus, for each hard signal event, the ADC end-of-conversion, a byte of data from the table is moved from flash to the switch array; therefore, the schedule is sequenced completely by DMA transactions, and the processor does not perform any work.

While the analog channels are scheduled via DMA, the data that exits the ADC must also be collected and collated for use according to the schedule. Again, DMA is employed for this task. Bins in a contiguous memory space within SRAM are defined for ADC data to be stored. DMA transaction descriptors are set up to sort the data into these bins based on where the schedule is. Thus, the TD array is aligned with the schedule so that data always arrives at the right place. For example, inverter output current reading and temperature readings will always show up in specific bins.

Figure 32. Analog Channel Scheduling and Data Gathering



Grid Synchronization

The PLL is integral to the operation of the inverter in that everything about DC/AC conversion is managed in sync with the AC line. All state management is synchronized to the line. All inversion-related control operations are synchronized to the line. The only item that is not directly synchronized to the line (although it could be) is the ripple cancellation control algorithm.

The PLL is operated slightly differently than that of other PLLs for this design. A line cycle is divided into 1024 slices, or 512 slices per half-sine. And the number of slices does not change. However, the distance between each slice is allowed to change. One key advantage is that the sine reference information is always the same. The granularity of the sine table can be set and maintained at all times. So, for any variation in the line, the harmonics, due to sine table granularity, are always the same.

Imagine the alternative, in which the number of slices is changed to generate the sine reference signal for varying frequency. In this scenario, the consistency of the sine information is varied. You could have 1000 points of sine information, 500 points of sine information or another number. The quality of the sine information is not consistent.

There is another advantage. Keeping the number of slices consistent implies that the sine table depth is consistent, and this is favorable for employing DMA in PSoC. The implementation is simple in code and takes a very low percentage of the overall processing. DMA automatically maintains the count/index into the sine table, and you don't need anything special to manage it other than to provide an event for the DMA to move on. In this situation, DMA is used to move sine information from a table in flash to a single RAM location. Therefore, a consuming function could be optimized to take information from a single RAM location, minimizing memory move operations by the core processor.

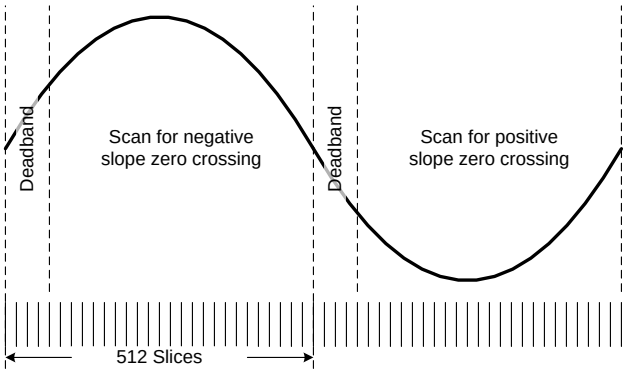
Only one half of the sine table is stored in flash. DMA is configured to generate a slice for every NRQ event. DMA manages the position in the table and, therefore, the count as well. The sine data is automatically transferred from flash to a single RAM location for consumption by any object that needs it. For example, the current control algorithm needs this information to shape the current injected into the grid.

Also adjoined with the sine data is additional information related to when to enable or disable the PSFB and when to fire the SCRB.

Grid Synchronization State Machine

The method employed is a simple sampled zero crossing detection technique. Figure 33 shows the operation.

Figure 33. PLL Line Cycle



A simple state machine is run to keep track of the line zero crossing. From this, the number of slices is captured from crossing to crossing. This information is saved and used to control the output. The state machine takes the following form:

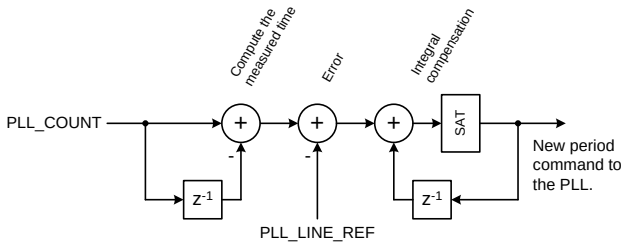
- State 1 – Scan for a zero crossing with a positive derivative of the incoming voltage. Thus, look at the voltage from one slice to the next and check for crossing zero while looking for a positive slope. When it is found, the counter is sampled. The count is used to keep track of the number of actual slices it took from the previous zero crossing to this one. The number of slices counted is compared to the 512 slices expected plus some offset. Adjustments are made to the period if necessary. The offset forces the PLL to constantly try to push the frequency off center. In addition the DMA is triggered to start the next sequence of 512 slices.
- State 2 – The voltage information is ignored for half of the line cycle. This is a blackout period to avoid false zero detects.
- State 3 – Scan for a zero crossing with a negative derivative of the incoming voltage. Thus look at the voltage from one slice to the next and check for crossing zero while looking for a negative slope. When it is found, the counter is sampled. The count is used to keep track of the number of actual slices it took from the previous zero crossing to this one. The number of slices counted is compared to the 512 slices expected, plus some offset. If necessary, make adjustments to the period. The offset forces the PLL to constantly try to push the frequency off center. In addition the DMA is triggered to start the next sequence of 512 slices.
- State 4 – The voltage information is ignored for half of the line cycle. This is a blackout period to avoid false zero detects.

PLL Control

The control loop is straightforward. Figure 34 shows a block view of the control. The distance, in terms of slices between each zero crossing is measured and compared with a reference. The reference is 512 plus some offset. The offset is employed to always keep the PLL pushing off frequency. If the microinverter were islanded, this feature would tend to drive the frequency beyond the shutdown frequency.

The error signal is fed into an integrator. Therefore, you could say that this is integral compensation. It is assumed that any frequency characteristics that could affect the stability of this simple loop are far out of the controllable region of interest. Therefore, the integral controller is sufficient for this design.

Figure 34. Basic PLL Control



Line Lock Detection

Because the control algorithm is so closely aligned with frequency measurement, line frequency reporting is combined in the same function. Filtering is used to integrate the jitter around zero detection to yield very accurate frequency detection. Lock detection could be employed around detecting zero error; however, in this case, the frequency requirements are very specific (i.e. either a 50-Hz or a 60-Hz grid), and therefore the grid frequency is used to indicate lock.

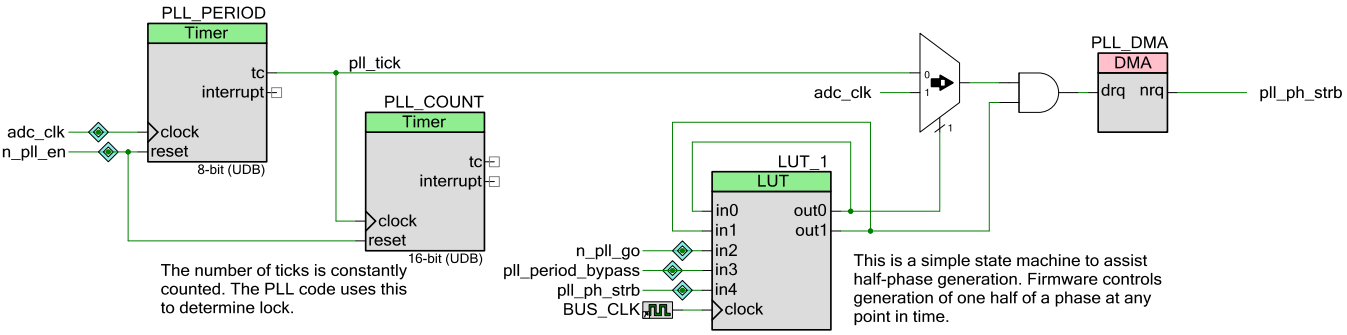
PLL Hardware

Figure 35 shows the PSoC hardware used for grid lock.

The key elements are as follows:

- PLL_PERIOD – The PLL_PERIOD is the base timer to control the distance between each slice. The control loop in firmware measures the actual distance and compares it against its reference to determine whether the period needs tuning up or tuning down.
- PLL_COUNT – A timer is used as a running counter to track the number of slices. The firmware takes samples of this counter at the zero crossings to determine total distance from one zero cross to the next.
- PLL_DMA – DMA is used to track the phase of the sine and to transfer the sine reference information from flash into a single RAM location.
- LUT_1 – This is a state machine to control the start of a cycle. One cycle is 512 slices. The firmware can kick off a cycle. The DMA will run through 512 slices, transferring continuously a sine reference into RAM. Through firmware, you have the option to accelerate the cycle at a very high rate to force an early finish.

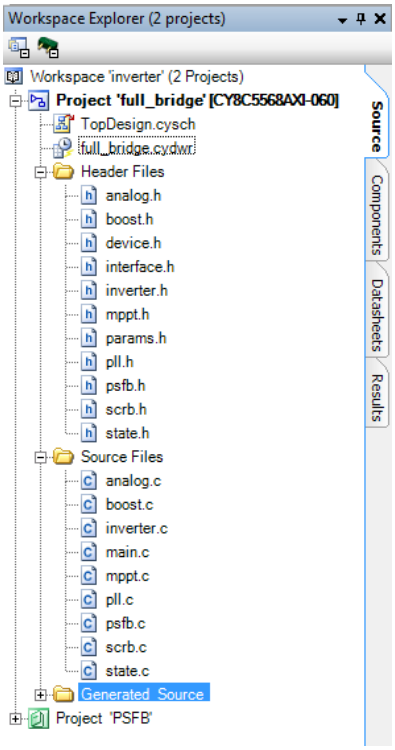
Figure 35. PLL Timing, Counting, and Sine Generation



Firmware Architecture in PSoC

Figure 36 shows a view of the project for the microinverter.

Figure 36. Project View



- main.c – This is the entry point into the code for this design.
- inverter.c/h – This is the integrating state machine object. The lowest level of execution flow is directed through this object, including some general state management. The major states of the inverter are operated from this object. All of the control systems and data-gathering systems are time-managed here.
- state.c/h – This object encapsulates the management of the entire inverter. All the major decisions are made here. For example, the inverter is held off unless the input voltage is within the operating range. Other examples include looking at voltages, current, temperature, and a few other conditions to decide starting, stopping, and how long to wait.
- pll.c/h – This is the PLL object, and it works with the PSoC hardware. The main purpose of the PLL object is to detect the presence of a line condition within normal line rates and lock in phase with that signal. Additional signals are generated, such as the sine data and SCRB firing angle, which are consumed by the appropriate objects.
- analog.c/h – This is the analog process-handling object. It has two major purposes, which are combined with PSoC's hardware capability. First, this object automatically schedules data gathering from multiple analog channels. Second, it provides some low-level digital filtering at lower data rates for other objects to consume.
- psfb.c/h – This is the PSFB startup and control object. This object is responsible for initializing the PSFB hardware and for processing the controls for programming the output current from the inverter to the AC grid.
- scrb.c/h – This object is responsible for managing the unfolding of the rectified current to create an AC waveform.
- mppt.c/h – This object contains the MPPT algorithm. It takes the input power and drives an output control variable, which is eventually consumed by the PSFB controls. The control output is continuously perturbed to determine the highest power it can find from the signal source.
- boost.c/h – This object processes the ripple control through the parallel synchronous boost converter. The control has two parts. One part controls the ripple, and the other, which is much slower, maintains a fixed duty cycle for the boost (thus managing the boost voltage).
- params.h – This file encapsulates the large number of parameters defined throughout the project. Most of the defined parameters are captured here to consolidate the large number of statically defined options into a single file. As a result, it is easier to change common conditions.

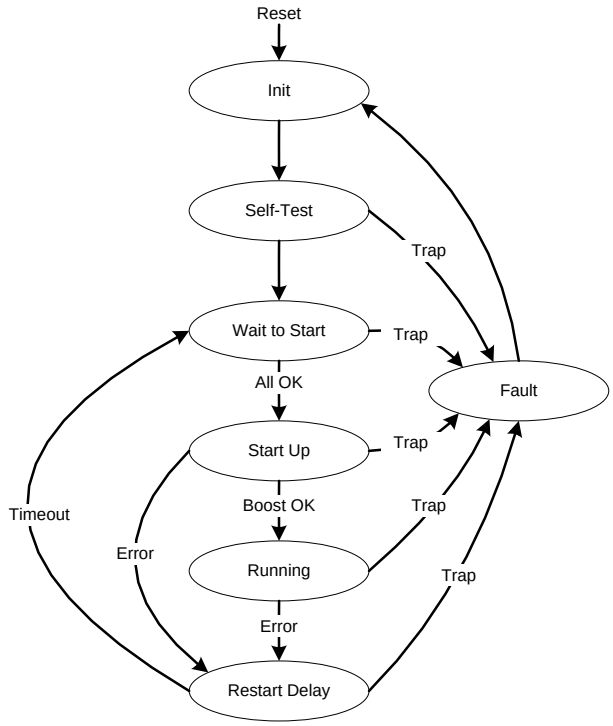
General State Management

The entire operation of the microinverter is guided by a state machine, which is implemented in the state.c object. Figure 37 shows the basic state flow.

- Init – This is a temporary state in which the inverter is completely reset and readied for operation.
- Self-Test – Begin a self-test sequence to ensure everything makes sense. If it doesn't, then something is wrong. Fault out to prevent problems. Note that this state is currently not used in this demonstration, but it is retained in the code to demonstrate the point that you can perform some self-checks. For example, you could check ADC values that are wildly out of bounds (i.e., cold solder joint). Self-checks could even include things such as checking RAM and flash consistency.
- Wait to Start – Remain in this state until the conditions are clear to start. For example, do not start if the PLL does not indicate proper lock or if voltages on the solar panel or grid are not within the operating range. If all conditions are good, then the ripple control and the boost are started.

- Startup – Start bringing up the system. While the system is starting, keep checking for conditions that would mandate a shutdown. For example, if the panel voltage drops while starting, discontinue startup.
- Running – At this point, the inverter is considered up and running. If the conditions do not look favorable to continue running, make the decision to transition to another mode of operation.
- Restart Delay – If there was a condition that mandated a shutdown, processing will pass through this state. This is nothing more than an exit event state available to process conditions at shutdown.

Figure 37. State Flow for the Microinverter



Control Board Hardware

The control card contains all the signal conditioning and feedback circuits required to properly operate the solar microinverter. In addition, the control card contains the physical layer for the Frequency Shift Keying (FSK)-based PLC modem. Attached with this application note are the PCB design files for the control card. The control card consists of the following:

- PSoC 5LP device for solar microinverter control and PLC communication
- Signal conditioning circuits for all feedback signals (both isolated and non-isolated)
- PLC transmit amplification and transmit filters
- PLC receive filters
- Analog signal conditioning and isolators
- Drivers for an SCR bridge

PSoC 5LP

This section includes the PSoC 5LP device along with the bypass capacitors and external oscillators.

Figure 38 shows the schematics, while Table 2 lists the bill of materials (BOM).

Figure 38. PSoC 5LP Device-Related Schematics

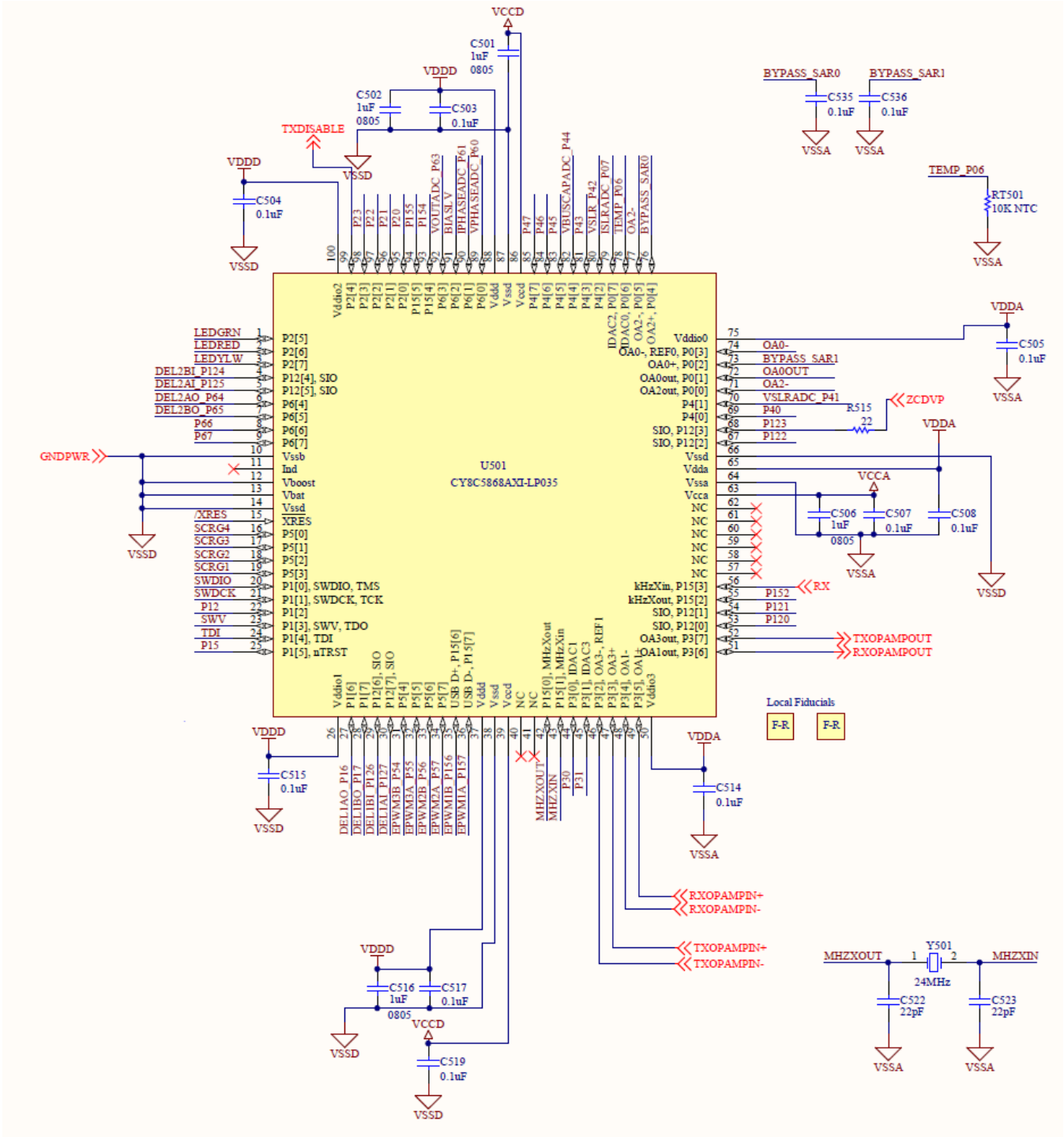


Table 2. PSoC 5LP Device-Related BOM

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
Capacitor Ceramic: 1-µF, 16-V, 10%, X7R 0603	C501, C502, C506, C516	4	1 µF	TDK Corp.	C1608X7R1C105K	445-1604-2-ND
Capacitor Ceramic: 0.1-µF, 10%, X7R 0603	C503, C504, C505, C507, C508, C514, C515, C517, C519, C535, C536	11	0.1 µF	TDK Corp.	C1608X7R1C104K	445-1317-2-ND
Capacitor Ceramic: 22-pF, 50-V, 5%, NP0 0603	C522, C523	2	22 pF	TDK Corp.	C1608C0G1H220J	445-1273-2-ND
Thermistor NTC: 10-kOhm, 5%, 0603	RT501	1	10 k NTC	Panasonic – ECG	ERT-J1VR103J	P10547TR-ND
IC PSoC 5LP: 32-bit, 256KB flash, 100-pin TQFP	U501	1	PSoC 5LP	Cypress Semiconductor Corp.	CY8C5868AXI-LP035	428-3228-ND
Crystal, 24.000-MHz, 20-pF SMD	Y501	1	24 MHz	ECS Inc.	ECS-240-20-5PX-TR	XC1255TR-ND

In addition to the decoupling capacitors, these are key components:

- C522, C523: These capacitors are required to bypass the reference voltages for SAR ADCs inside the PSoC 5LP device. Please refer to the SAR ADC for more information.
- Y502: The PSoC 5LP device uses a 24-MHz crystal to generate a precise 48-MHz bus clock for the PLC modem. This crystal device is not required for standalone solar microinverter operation.
- RT501: The system ambient temperature is sensed by driving a current into the NTC thermistor using an onboard IDAC. The voltage dropped across the thermistor is sensed by the ADC and converted to a temperature value by the firmware.

Reference Generation

The control board design uses a 1.24-V reference to sense analog signals. Two reference voltages are available on the control board.

- A 1.24-V reference is used for differential sensing on the isolated side. This voltage is generated on the control board.
- A second 1.24-V reference is used for differential sensing on the control side. The circuit on the power board generates this reference voltage.

Figure 39. Low-Voltage Reference Generation for Differential Sensing on the Isolated Side

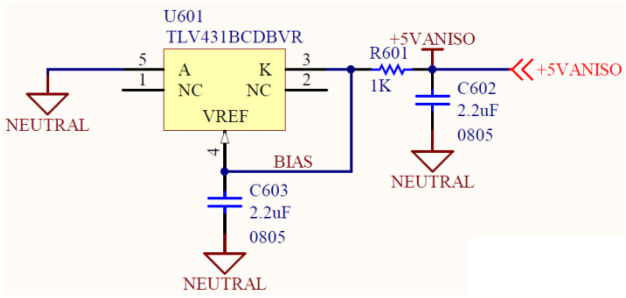


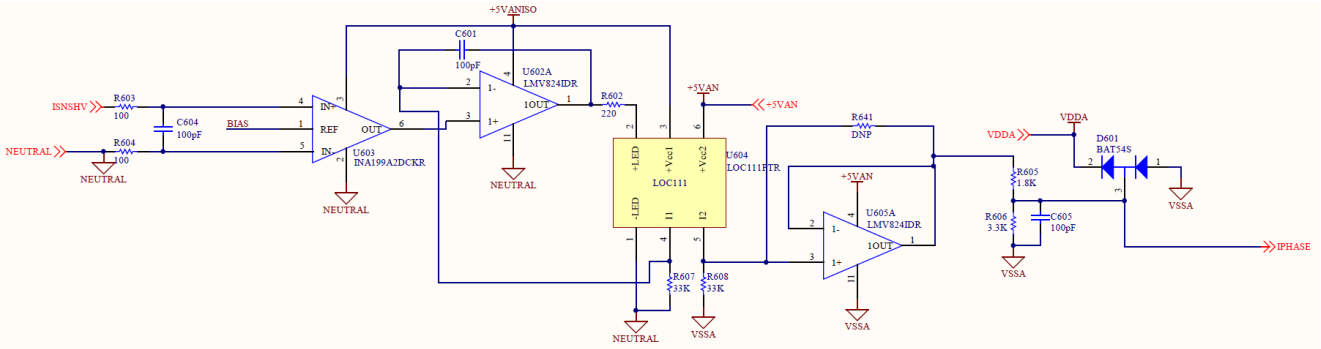
Figure 39 shows the schematic for the reference generation circuit on the isolated side. This circuit is powered by the isolated 5-V rail.

Table 3 lists the BOM for the reference generation circuit.

Table 3. Reference Generation Circuit BOM

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
Capacitor Ceramic, 2.2-µF 25-V, 20% X5R 0805	C602, C603	2	2.2 µF	TDK Corp.	C2012X5R1E225M/1.25	445-7630-2-ND
Resistor: 1.0-kOhm, 1/10-W, 1% 0603	R601	1	1 k	Panasonic - ECG	ERJ-3EKF1001V	P1.00KHTR-ND
1.024-V, 0.5% Precision Shunt Reference	U601	1	TLV431	Texas Instruments	TLV431BCDBVR	296-17568-1-ND

Figure 40. Inverter Phase Current Sensing and Isolation Circuit Schematics



AC Current Sensing

The inverter phase current is sensed by a 5-mOhm current sense resistor on the power board and is fed to the control board. This current-equivalent voltage signal is then amplified by a differential amplifier and is DC offset to the reference voltage. Components R603, R604, C604, and U603 form this differential amplifier circuit.

The opto-isolator U604 provides necessary ohmic isolation from the AC side. U602, U604, C601, and R607 form a negative feedback loop. The opto-isolator features an infrared LED optically coupled to two matched phototransistors.

The input phototransistor is used to generate a control signal that provides a mechanism to compensate the LEDs' non-linear characteristics. The output phototransistor provides an output signal that is linear with respect to the LED current and that is isolated from the input signal.

The output of the isolator is buffered by a unity gain voltage follower: the U605. The voltage divider formed by R605 and R606 brings down the output of U605 to a level that the PSoC 5LP pins can accept. D601 provides the necessary protection to the pin.

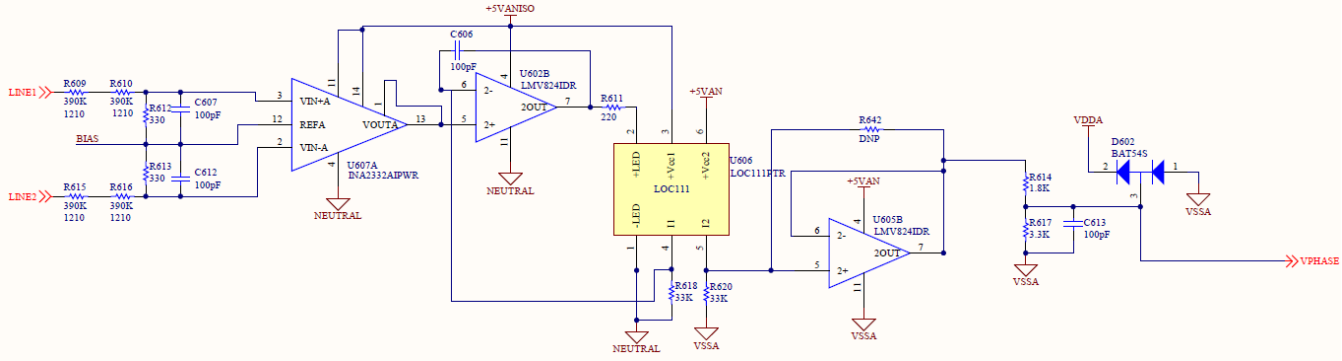
Table 4 lists the BOM for the inverter current sensing and isolation circuit.

Table 4. Inverter Phase Current Sensing Circuit BOM

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
Capacitor Ceramic: 100-pF, 50-V, 5% NP0 0603	C601, C604, C605	3	100 pF	TDK Corp.	C1608C0G1H101J	445-1281-2-ND
Diode Schottky: 30-V 200-mA SOT-23	D601	1	BAT54S	Fairchild Semiconductor	BAT54S	BAT54SFSTR-ND
Resistor: 220–Ohm, 1/10-W, 1% 0603	R602	1	220	Panasonic - ECG	ERJ-3EKF2200V	P220HTR-ND
Resistor: 100-Ohm, 1/10-W, 1% 0603	R603, R604	2	100	Panasonic - ECG	ERJ-3EKF1000V	P100HTR-ND

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
Resistor: 1.80-kOhm, 1/10-W, 1% 0603	R605	1	1.80 k	Panasonic - ECG	ERJ-3EKF1801V	P1.80KHTR-ND
Resistor: 3.30-kOhm, 1/10-W, 1% 0603	R606	1	3.3 k	Panasonic - ECG	ERJ-3EKF3301V	P3.30KHTR-ND
Resistor: 33-kOhm, 1/10-W, 1% 0603	R607, R608	2	33 k	Panasonic - ECG	ERJ-3EKF3302V	P33.0KHTR-ND
IC general-purpose opamp Rail-Rail 5.5 MHz	U602, U605	2	LMV824IDR	Texas Instruments	LMV824IDR	296-18466-2-ND
Opto-coupler Transistor	U604	1	LOC111	Clare	LOC111PTR	CLA118TR-ND
IC Current Shunt Monitor	U603	1	INA199A2DCKR	Texas Instruments	INA199A2DCKR	296-27331-2-ND

Figure 41. AC Line Voltage Sensing and Isolation Circuit Schematics



AC Voltage Sensing

Figure 41 shows the schematics for AC line voltage sensing and the isolation circuit. R609, R610, R615, R616, R612, R613, C607, C612, and U607 form the differential amplifier that senses the AC line voltage differentially and provides an output that is offset by reference voltage.

C606, R611, R618, and U602 provide a stabilized control loop for the LED in the opto-isolator U606. The output of the isolator is buffered by a unity gain voltage follower: the U605. The voltage divider formed by R614 and R617 brings down the output of U605 to a level that the PSoC 5LP pins can accept. D601 provides the necessary protection to the pin.

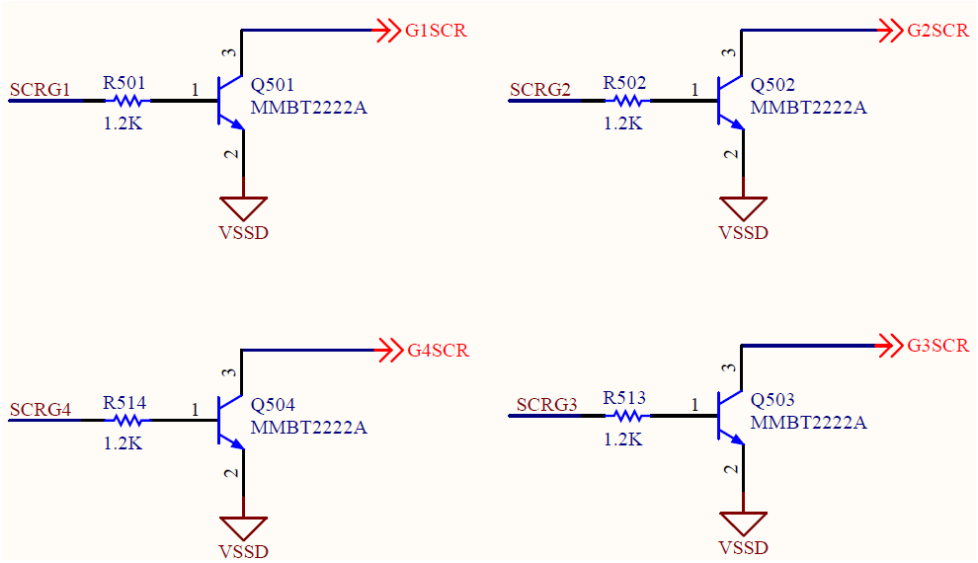
Table 5 lists the BOM for the AC line voltage sensing and isolation circuit.

Table 5. AC Line Voltage Sensing and Isolation Circuit BOM

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
Capacitor Ceramic: 100-pF, 50-V, 5% NP0 0603	C601, C606, C607, C612, C613	3	100 pF	TDK Corp.	C1608C0G1H101J	445-1281-2-ND
Diode Schottky: 30-V, 200-mA	D602	1	BAT54S	Fairchild Semiconductor	BAT54S	BAT54SFSTR-ND
Resistor: 390-kOhm, 1/10-W, 1% 0603	R609, R610, R615, R616	4	390 k	Panasonic - ECG	ERJ-14NF3903U	P390KAATR-ND
Resistor: 220-Ohm, 1/10-W, 1% 0603	R611	1	220	Panasonic - ECG	ERJ-3EKF2200V	P220HTR-ND

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
Resistor: 330-Ohm, 1/10-W, 1% 0603	R612, R613	2	330	Panasonic - ECG	ERJ-3EKF3300V	P330HTR-ND
Resistor: 1.80-kOhm, 1/10-W, 1% 0603	R614	1	1.80 k	Panasonic - ECG	ERJ-3EKF1801V	P1.80KHTR-ND
Resistor: 3.30-kOhm, 1/10-W, 1% 0603	R617	1	3.3 k	Panasonic - ECG	ERJ-3EKF3301V	P3.30KHTR-ND
Resistor: 33-kOhm, 1/10-W, 1% 0603	R618, R620	2	33 k	Panasonic - ECG	ERJ-3EKF3302V	P33.0KHTR-ND
IC general-purpose opamp Rail-Rail 5.5-MHz	U602, U605	2	LMV824IDR	Texas Instruments	LMV824IDR	296-18466-2-ND
Opto-coupler Transistor	U606	1	LOC111	Clare	LOC111PTR	CLA118TR-ND
IC Instrumentation opamp Rail-Rail 2-MHz	U607	1	INA2332AIPWR	Texas Instruments	INA2332AIPWR	INA2332AIPWRTR-ND

Figure 42. SCR Bridge Pre-Driver



SCRB Drivers

The transistors Q501, Q502, Q503, and Q504, along with resistors R501, R502, R514, and R515, form the SCR pre-driver circuit. The trigger pulses that originate from the PSoC 5LP device are current-amplified and then fed to the isolated SCR drivers on the power board.

Figure 42 shows the related schematics and the BOM.

Table 6. SCR Bridge Pre-Drivers BOM

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
General-Purpose NPN Transistor: 1-A	Q501, Q502, Q503, Q504	4	MMBT2222A	Fairchild Semiconductor	MMBT2222A	MMBT2222AFSTR-ND
Resistor: 1.2-kOhm, 1/10-W, 1% 0603	R501, R502, R514, R515	4	1.2 k	Panasonic - ECG	ERJ-3EKF1201V	P1.20KHTR-ND

Figure 43. PSFB Modulation Delay Generation Circuit

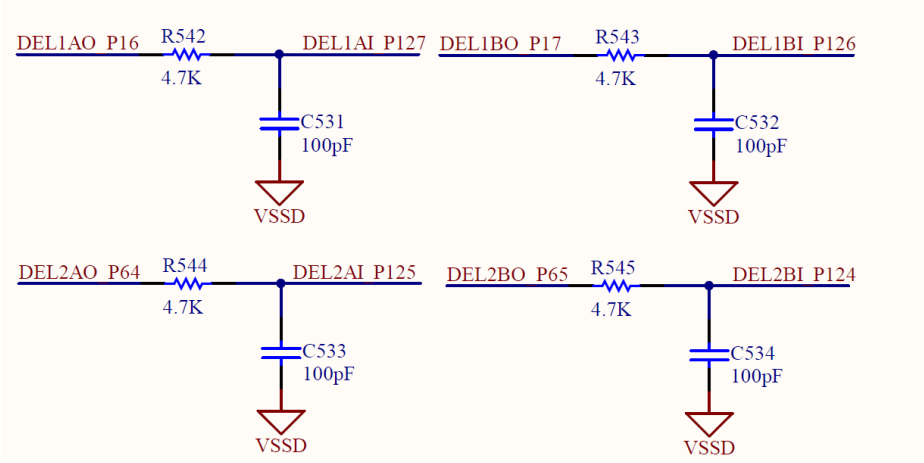


Table 7. PSFB Modulation Delay Generation Circuit BOM

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
Capacitor Ceramic: 100-pF, 50-V, 5% NP0 0603	C531, C532, C533, C534	4	100 pF	TDK Corp.	C1608C0G1H101J	445-1281-2-ND
Resistor: 4.7-kOhm, 1/10-W, 1% 0603	R542, R543, R544, R545	4	4.7 k	Panasonic - ECG	ERJ-3EKF4701V	P4.70KHTR-ND

PSFB Modulation Delay

Figure 43 shows the RC delay circuits used to generate necessary delays to turn ON each individual switch of the full-bridge. Table 7 lists the BOM for the same circuit.

The special input/output (SIO) pins on the PSoC 5LP device generate the necessary delay. The comparator on each SIO pin is used to program the delay with the exponential controlled by the RC network.

If the SIO comparator trigger point is set to 50% of the VDDIO value driving the pin, then,

Equation 7 $$t_{delay} = (R)(C)\ln(2)$$

Therefore, you can program each edge of the PWM driving the PSFB individually with a simple RC network. This individual programmability is important because ZVS is achieved on only one phase of the bridge. This time of delay control also helps to match different propagation delays through the high-side/low-side drivers.

For more information on how to use the SIOs, please refer to AN60580 – SIO Tips and Tricks in PSoC® 3 / PSoC 5LP.

Signal Conditioning Circuit

Figure 44 shows the schematics of analog signal conditioning circuits. Table 8 lists their BOM.

The analog signal conditioning circuits are in place to buffer and filter the analog signals before taking them as input to the PSoC device. U502 and U503 are configured to buffer the analog signals.

In addition, the voltage from the solar panel is buffered by the opamp inside the PSoC 5LP device.

Figure 44. Signal Conditioning Circuits

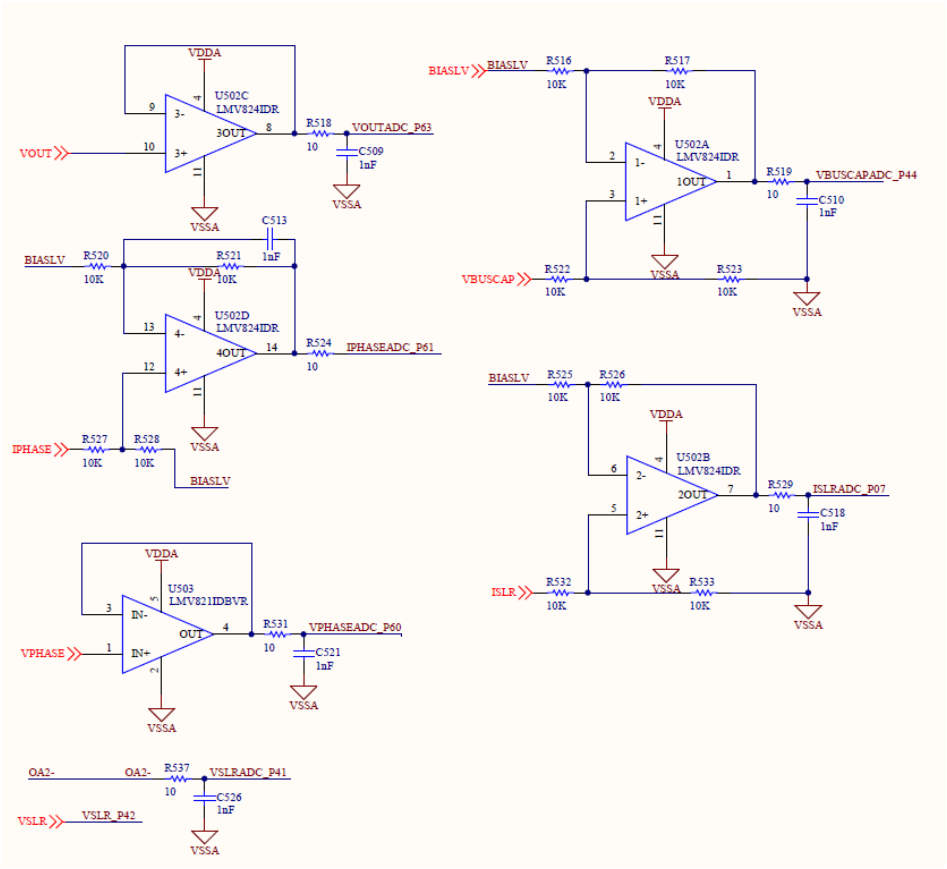


Table 8. Signal Conditioning Circuit BOM

Description	Designator	Qty	Value	Manufacturer	Manufacturer Part #	Vendor Part #
Capacitor Ceramic: 1-nF, 50-V, 5% NP0 0603	C509, C510, C513, C518, C521, C526	6	1 nF	TDK Corp.	C1608C0G1H102J	445-1293-2-ND
Resistor: 10.0-Ohm, 1/10-W, 1% 0603 SMD	R518, R519, R524, R529, R531, R537	6	10	Panasonic - ECG	ERJ-3EKF10R0V	P10.0HTR-ND
Resistor: 10.0-kOhm, 1/10-W, 1% 0603 SMD	R516, R517, R520, R521, R522, R523, R525, R526, R527, R528 R532, R533	12	10 kOhm	Panasonic - ECG	ERJ-3EKF1002V	P10.0KHTR-ND
IC general-purpose opamp Rail-Rail, 5.5-MHz	U502	1	LMV824IDR	Texas Instruments	LMV824IDR	296-18466-2-ND
IC general-purpose opamp Rail-Rail, 5.5-MHz	U503	1	LMV821IDR	Texas Instruments	LMV821IDBVR	296-18461-2-ND

Related Application Notes

AN77759 – Getting Started with PSoC 5LP

AN60580 – SIO Tips and Tricks in PSoC 3 / PSoC 5LP

AN76439 – PSFB Modulation and Control

AN76458 – PSoC 5LP Powerline Communication Solution

AN82156 – UDB Datapath Programming

AN82250 – Verilog Programming

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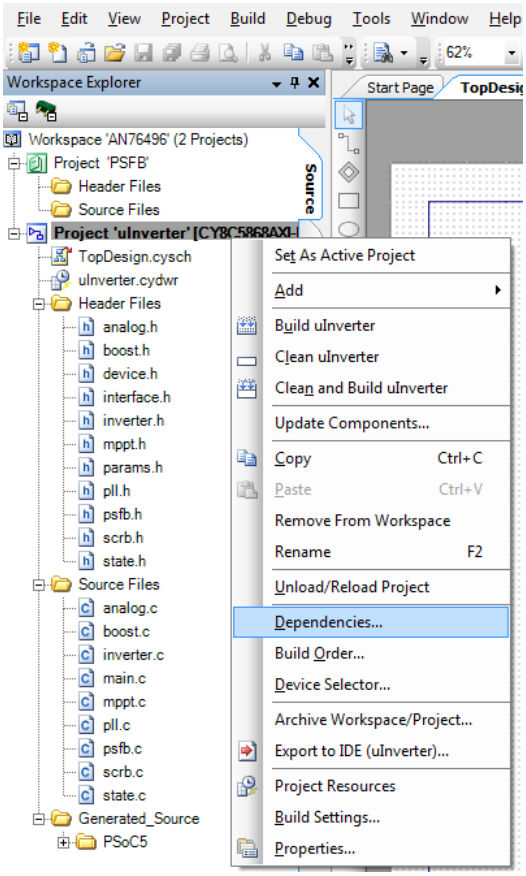
Appendix A: Using the PSFB Component in Your Project

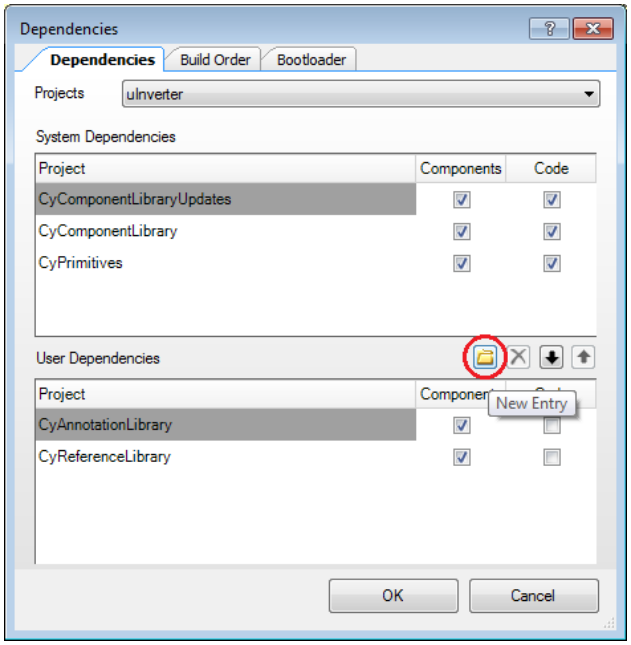
To add the PSFB component to your project, you must add it as a dependency. To do this, right-click on the project's name in Workspace Explorer of the PSoC Creator window. Select the Dependencies option in the pop-up menu, as shown in Figure 45.

Figure 45. Select Dependencies Option



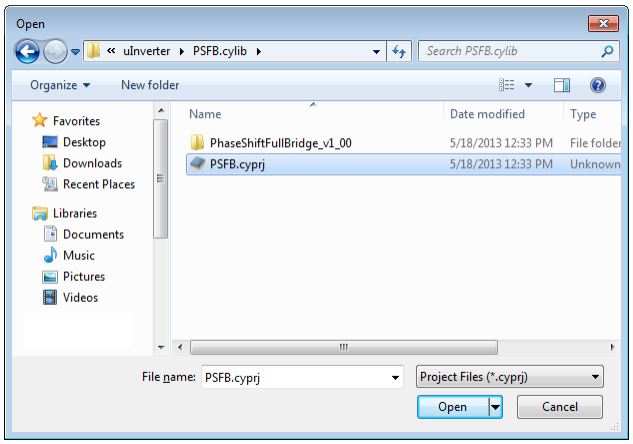
When the Dependencies dialog opens, click the folder icon for User Dependencies, as shown in Figure 46.

Figure 46. Adding a User Dependency



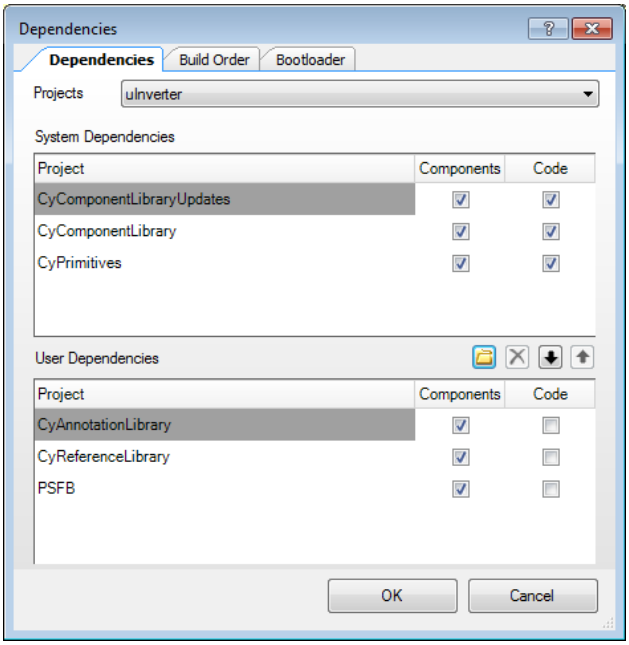
Navigate to the folder containing the library where the PSFB component resides. In this case, it is in the folder PSFB.cylib. Select the file PSFB.cyprj, as Figure 47 shows.

Figure 47. Select the PSFB Component



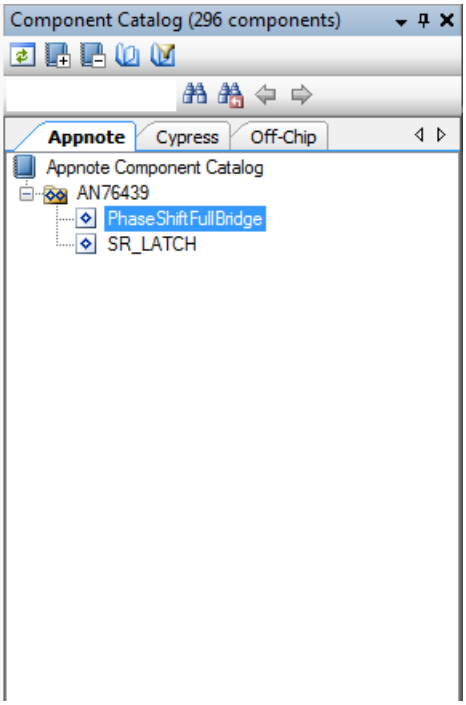
After the PSFB component is added to the project, you will see it in the Dependencies tab, as Figure 48 shows.

Figure 48. PSFB Component Added to Project



After the component is added to the project, it will appear in the Component Catalog of PSoC Creator, as Figure 49 shows. It will be listed in the Appnote tab under Appnote Component Catalog/AN76439 entry.

Figure 49. PSFB Component in the Catalog



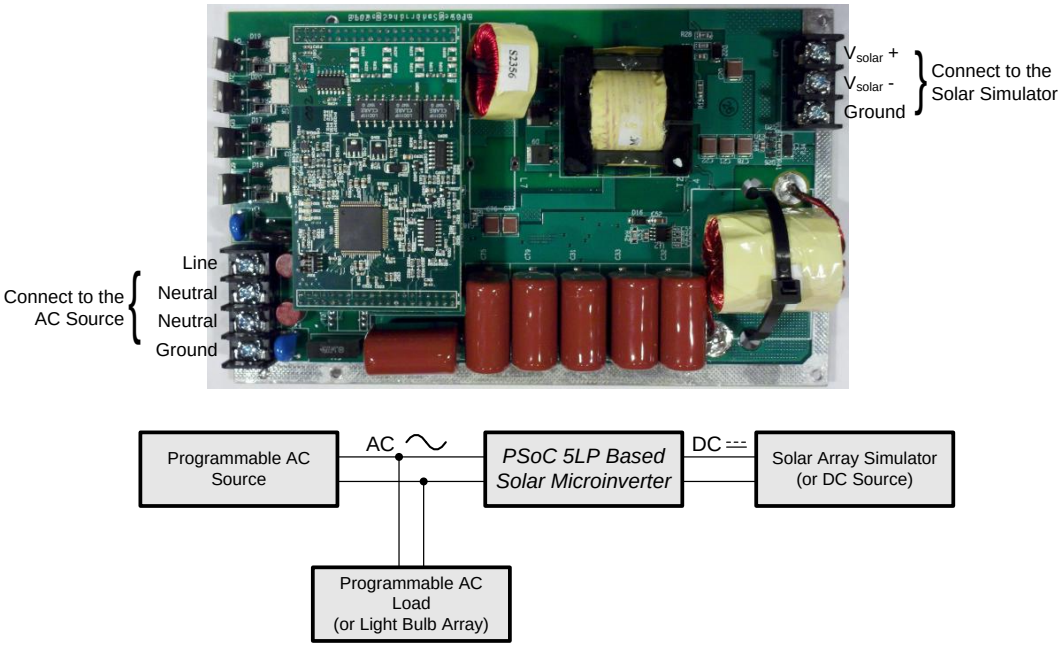
Appendix B: PSoC 5LP Microinverter Demonstration Quick Setup Guide

PSoC® 5LP MICROINVERTER DEMONSTRATION QUICK SETUP GUIDE

This guide provides quick setup instructions for evaluating the PSoC 5LP Based Microinverter Demonstration. Note that the microinverter is a complex design that operates at high voltage levels. These voltage levels are potentially hazardous when not properly handled. Use extreme caution when working with this demonstration! This guide assumes that you are very familiar with such high-voltage equipment and the safety requirements necessary when working with and handling such equipment.

1. Some equipment is necessary for the evaluation of the microinverter. Note that it is assumed the user of this demonstration will have access to such equipment, is proficient at using such equipment, and is knowledgeable with testing similar power designs. The equipment needed is:
   - Programmable AC source, ≥ 1.5kVA @ 300VAC
   - Programmable AC load, ≥ 500W @ 300V
   - Programmable Solar Array Simulator, ≥ 500W @ 60V

   Alternatively, for a simpler demonstration it is possible to eliminate some of the more specialized equipment above for a slightly more economical functional test. Such a configuration would require:
   - Programmable AC source, ≥ 1.5kVA @ 300VAC
   - An array of five 100W @ 120V light bulbs
   - Programmable DC source with constant current limit, ≥ 500W @ 60V
2. Connect the AC source to the AC input on the inverter. The inverter is pre-configured to support 120VAC (±2.0%) input with a line frequency of 60Hz (±0.2%). By default, voltages and/or operating frequencies that are outside the tolerance will prevent the inverter from starting up.
3. Connect the AC load (or light bulb array) to the AC source. The load must be greater than the highest output power configuration for the solar array simulator (or DC source). In essence, this is the simulated load on the grid. While the inverter is in operation, it will take over the energy supplied to the load by the simulated grid (the AC source).
4. Connect the solar array simulator to the DC side of the solar microinverter. The microinverter is designed to handle as much as 60V on the input. Do not exceed this! The inverter will convert up to 300W at its input. If the peak power is lower than the maximum, then the inverter will track to maximum power that can be sourced from the solar simulator (or DC source).



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Document History

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**	4010299	ROSS	05/24/2013	New Spec.
*A	4479494	SNVN	08/20/2014	Added a note to the abstract.
*B	5701647	AESATMP9	04/26/2017	Updated logo and copyright.

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