MB170 IDTV
SERVICE MANUAL

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IMPORTANT

Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17MB170 main board is driven by MTK SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

This board can be driven 50Hz UHD panels.

Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Rich internet connectivity and completed digital home network solution
- Dual-stream decoder for 3D contents
- Multi-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM (for connected option)

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Back AV (CVBS, R/L_Audio)
- 1 PC input(Common)
- 4x HDMI inputs (with ARC option from 2nd or 3rd input)
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2 USB(2X Side) and 1x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 External Keypad/Tact Switch

2. T/T2/C/A TUNER (U118)

Description:

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Features:

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
- 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™,DTMB
- Lowest BOM for a hybrid TV tuner
  - No balun, SAW filters, or external inductors required
  - Increased ESD protection on 4pins
- Best-in-class real-world reception
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - Integrated 1.8 V LDO for 3.3 V singlesupply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant

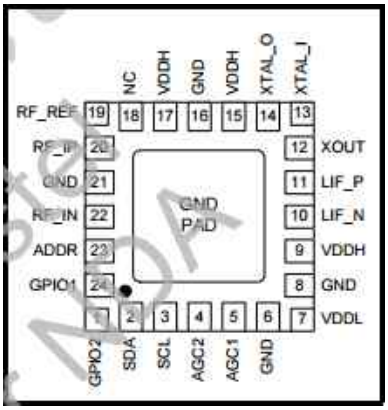


Figure 1: Si2151 Pin description

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I^2C data input/output
3	SCL	I	I^2C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground
17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I^2C address select
24*	GPIO1	I/O	General purpose input/output #1
***Note:** Pin should be left floating if unused.			

3. S/S2 TUNER (U3) OPTIONAL

Description

M88TS6011 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS6011 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS6011 requires only one crystal, one matching network, and a few external capacitors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS6011 can be configured via a 2-wire serial bus. The chip is available in a 16-pin QFN package.

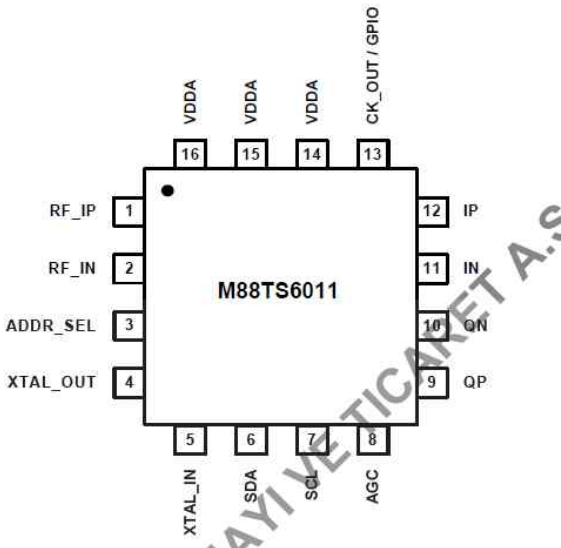
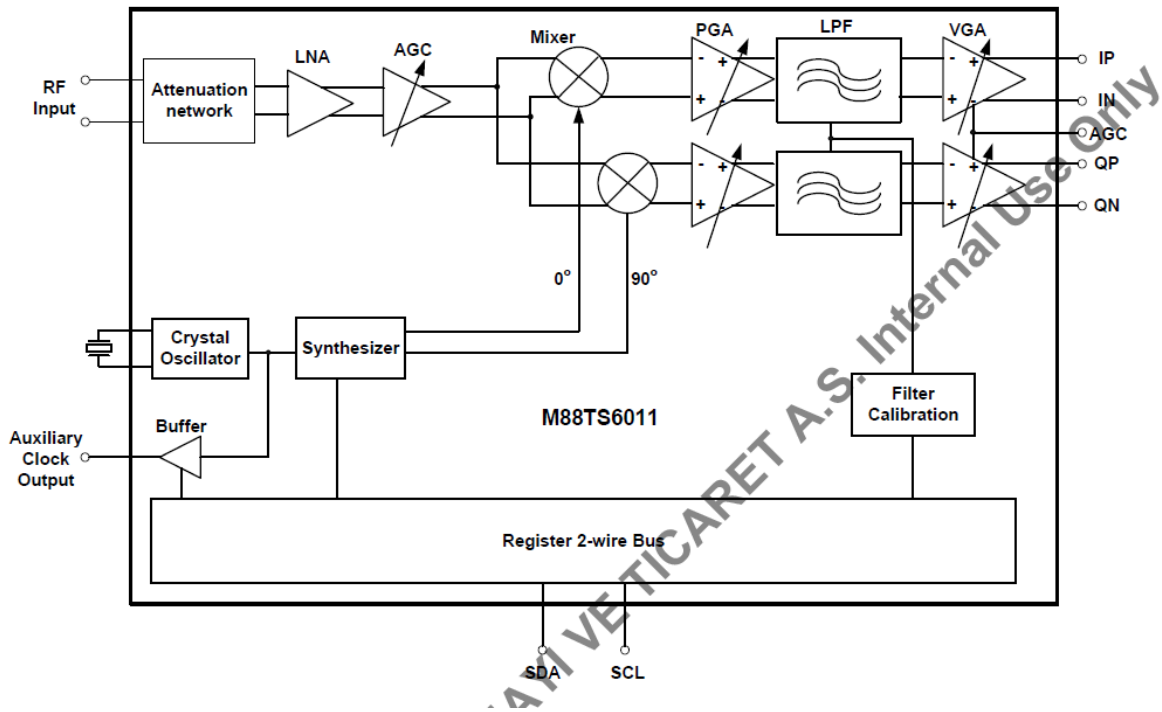


Figure 2: Pin description

Features

- Single-chip tuner
- Compliant with DVB-S/S2 and ABS-S standards
- Support QPSK, 8PSK, 16APSK and 32APSK
- Direct-conversion from L-band to baseband
- Symbol rate: 1 to 45 Msymbol/s
- Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter
- Integrated baseband filters: 6 MHz to 40 MHz bandwidth
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation removes external loop filters
- Excellent immunity to strong adjacent undesired channels
- Integrated clock driver provides auxiliary clock output for other devices
- Support sleep mode
- 2-wire serial bus with 3.3 V compatible logic levels
- Power supply: +3.3 V
- Package:16-pin E-PAD QFN
- RoHS compliant

Block Diagram



4. AUDIO AMPLIFIER STAGES

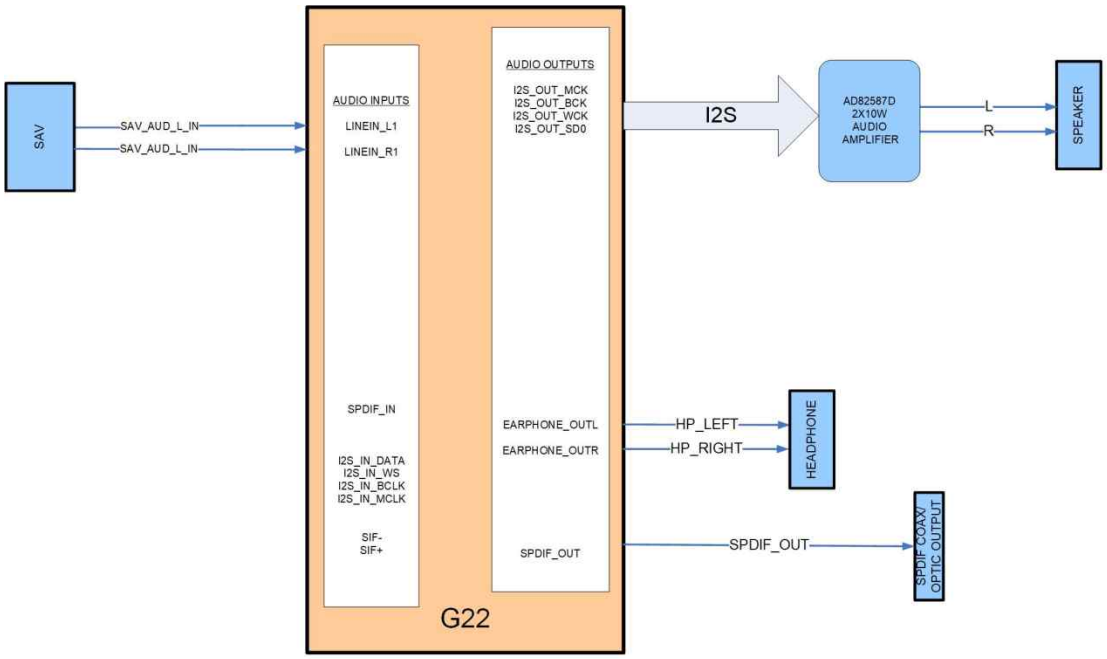


Figure 3: The block diagram of the audio part

MAIN AMPLIFIER (U123) (8W/10W/12W OPTIONS)

Description

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4 ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82587D's input format selection, DRC (dynamic range control), mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
  - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  - 64x~256x Fs for 128kHz /176.4kHz/192kHz

- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  - 10W x 2ch into 8_ @ 0.16% THD+N
  - 15W x 2ch into 8_ @ 0.18% THD+N
  - 20W x 2ch into 8_ @ 0.24% THD+N

- Loudspeaker output power for Mono@ 24V
  - 20W x 1ch into 4_ @ 0.17% THD+N
  - 30W x 1ch into 4_ @ 0.2% THD+N
  - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
  - Volume control (+24dB~-103dB, 0.125dB/step)
  - Dynamic range control
  - Power clipping
  - Channel mixing
  - User programmed noise gate with hysteresis window
  - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

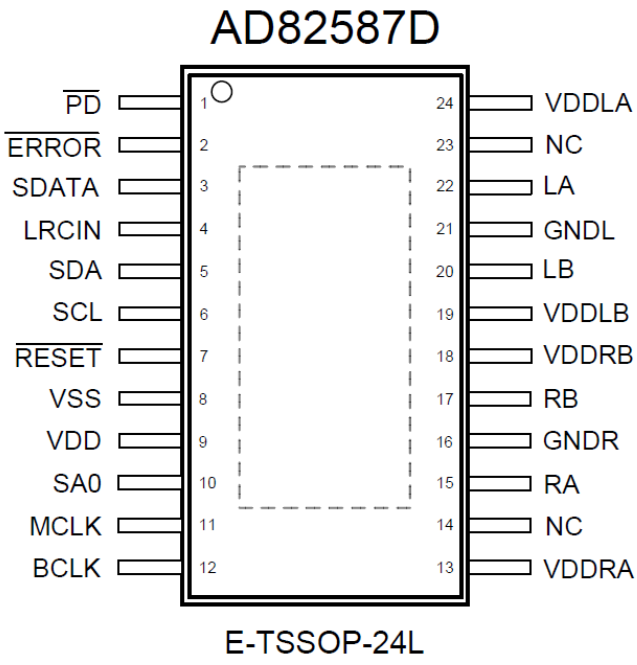


Figure 4: Pin description

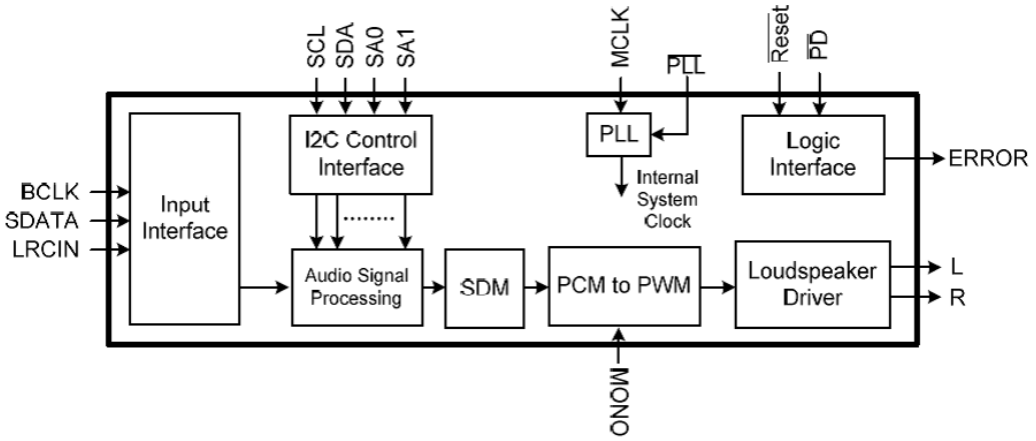


Figure 5: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Table 2: Recommended Operating Conditions

5. POWER STAGE

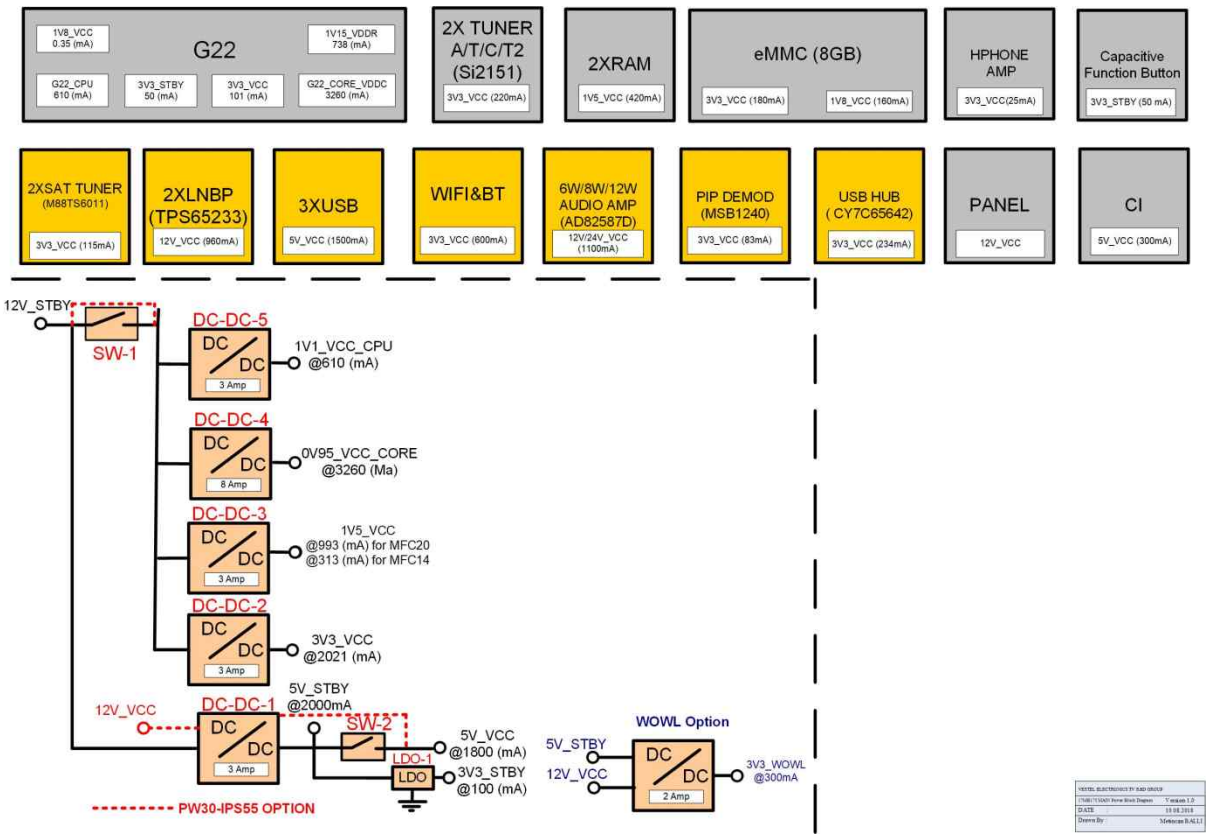


Figure 6: Power Block Diagram

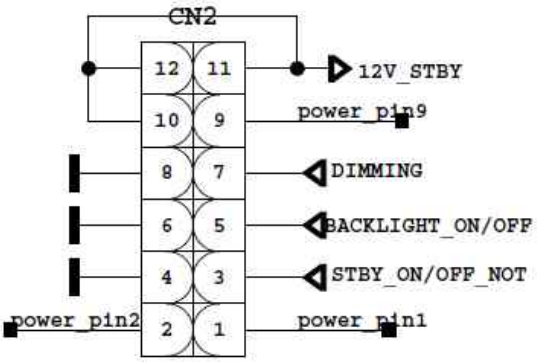


Figure 7: Power Socket and Power Options

Power socket is used for taking 12V_STBY voltage which is produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. Power socket pinning is shown in above figure.

12V_STBY is converted several different voltages on the mainboard which are shown in below figure.

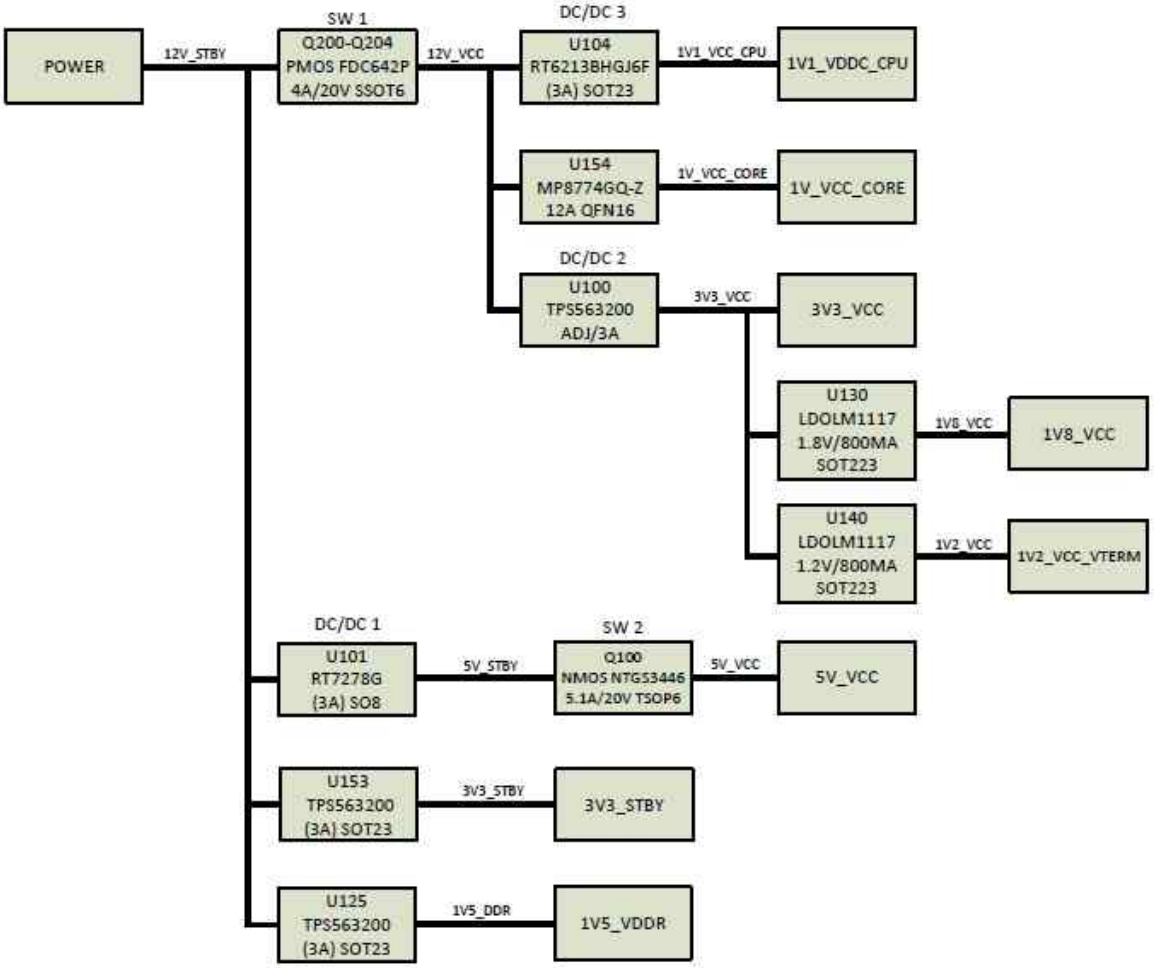


Figure 8: Power Block Diagram

List of the components:

- SW-1(Q200) → FDC642P 4A/20V
- SW-2(Q100) → NTGS3446 5.1A/20V
- DC-DC-1(U101) → RT7278G ADJ/3A
- DC-DC-2(U100) → TPS563200 ADJ/3A
- DC-DC-3(U104) → RT6213BHGJ6F ADJ/3A
- DC-DC-4(U153) → TPS563200 ADJ/3A
- DC-DC-5(U125) → TPS563200 ADJ/3A
- DC-DC-6(U154) → MP8774GQ-Z 12A QFN16
- LDO-1(U130) → LDO LM1117
- LDO-2(U140) → LDO LM1117

A. FDC642P (Q200)

Single P-Channel 2.5V Specified PowerTrench® MOSFET
-20 V, -4.0 A, 65 mΩ

Features

- Max $r_{DS(on)}$ = 65 mΩ at V_{GS} = -4.5 V, I_D = -4.0 A
- Max $r_{DS(on)}$ = 100 mΩ at V_{GS} = -2.5 V, I_D = -3.2 A
- Fast switching speed
- Low gate charge (11nC typical)
- High performance trench technology for extremely low $r_{DS(on)}$
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1 mm thick)
- Termination is Lead-free and RoHS Compliant

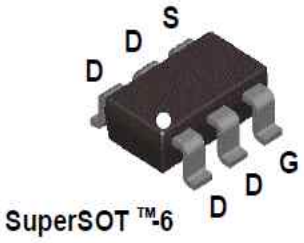
General Description

This P-Channel 2.5V specified MOSFET is produced using Fairchild's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the larger packages are impractical.

Applications

- Load switch
- Battery protection
- Power management



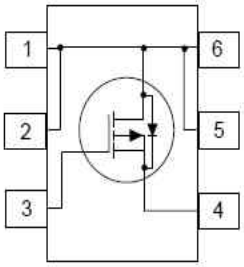


Figure 9: Pin description

B. NTGS3446 (Q100)

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- IDSS Specified at Elevated Temperature
- Pb−Free Package is Available

Applications

- Power Management in portable and battery−powered products, i.e. computers, printers, PCMCIA cards, cellular and cordless
- Lithium Ion Battery Applications
- Notebook PC

PIN ASSIGNMENT

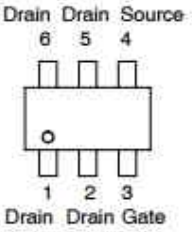


Figure 10: Pin description

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	V
Gate–to–Source Voltage	V_{GS}	±12	V
Thermal Resistance Junction–to–Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 244 0.5 2.5 10	 °C/W W A A
Thermal Resistance Junction–to–Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 128 1.0 3.6 14	 °C/W W A A
Thermal Resistance Junction–to–Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Drain Current – Continuous @ T_A = 25°C – Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 62.5 2.0 5.1 20	 °C/W W A A
Source Current (Body Diode)	I_S	5.1	A
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

Table 3: Maximum ratings

C. RT7278G (U101)

General Description

The RT7278 is a synchronous DC/DC step-down converter with Advanced Constant On-Time (ACOT™) mode control. It achieves high power density to deliver up to 3A output current from a 4.5V to 18V input supply. The proprietary ACOT™ mode offers an optimal transient response over a wide range of loads and all kinds of ceramic capacitors, which allows the device to adopt very low ESR output capacitors for ensuring performance stabilization. In addition, RT7278 keeps an excellent constant switching frequency under line and load variation and the integrated synchronous power switches with the ACOT™ mode operation provides high efficiency in whole output current load range. Cycle-by-cycle current limit provides an accurate protection by a valley detection of low side MOSFET and external soft-start setting eliminates input current surge during startup. Protection functions also include output under voltage protection, output over voltage protection, and thermal shutdown.

Features

- **ACOT™ Mode Enables Fast Transient Response**
- **4.5V to 18V Input Voltage Range**
- **3A Output Current**
- **60mΩ Internal Low Site N-MOSFET**
- **Advanced Constant On-Time Control**
- **Support All Ceramic Capacitors**
- **Up to 95% Efficiency**
- **700kHz Switching Frequency**
- **Adjustable Output Voltage from 0.765V to 8V**
- **Adjustable Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Input Under Voltage Lockout**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

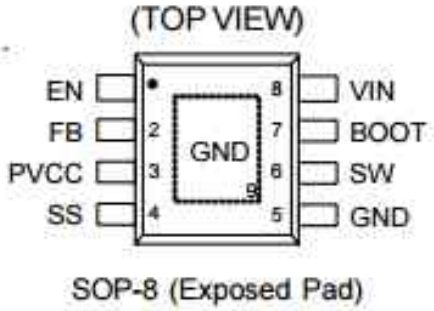


Figure 11: Pin Assignment

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
2	FB	Feedback Voltage Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback threshold voltage is 0.765V typically.
3	PVCC	Regulator Output for Internal Circuit. Connect a 1μF capacitor to GND to stabilize output voltage.
4	SS	Soft-Start Time Setting. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of V_{OUT} to 2.6ms.
5, 9 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	SW	Switch Node. Connect this pin to an external L-C filter.
7	BOOT	Bootstrap Supply for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
8	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	1.5	10	μA
Quiescent Current		I_Q	V_{EN} = 3V, V_{FB} = 1V	--	0.7	--	mA
Logic Threshold							
EN Input Voltage	Logic-High			2	--	18	V
	Logic-Low			--	--	0.4	
V_{FB} Voltage and Discharge Resistance							
Feedback Threshold Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 18V	0.757	0.765	0.773	V
Feedback Input Current		I_{FB}	V_{FB} = 0.8V	-0.1	0	0.1	μA
V_{PVCC} Output							
V_{PVCC} Output Voltage		V_{PVCC}	6V ≤ V_{IN} ≤ 18V, 0 < I_{PVCC} < 5mA	4.7	5.1	5.5	V
Line Regulation			6V ≤ V_{IN} ≤ 18V, I_{PVCC} = 5mA	--	--	20	mV
Load Regulation			0 < I_{PVCC} < 5mA	--	--	100	mV
Output Current		I_{PVCC}	V_{IN} = 6V, V_{PVCC} = 4V	--	110	--	mA

D. TPS563200 (U100, U153, U125)

1 Features

- TPS562200 - 2A converter with Integrated 122 mΩ and 72 mΩ FETs
- TPS563200 - 3A converter with Integrated 68 mΩ and 39 mΩ FETs
- D-CAP2™ Mode Control for Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- 650 kHz Switching Frequency
- Advanced Eco-mode™ Pulse-skip
- Low Shutdown Current Less than 10 µA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-By-Cycle Overcurrent Limit
- Hiccup-Mode Undervoltage Protection
- Non-latch OVP, UVLO and TSD Protections
- Fixed Soft Start: 1 ms

2 Applications

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

3 Description

The TPS562200 and TPS563200 are simple, easy-to-use, 2 A and 3 A synchronous step-down (buck) converters in 6 pin SOT-23 package.

The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

TPS562200 and TPS563200 operate in Advanced Eco-mode, which maintains high efficiency during light load operation. The devices are available in a 6-pin 1.6mm x 2.9mm SOT (DDC) package, and specified from –40°C to 85°C of ambient temperature.

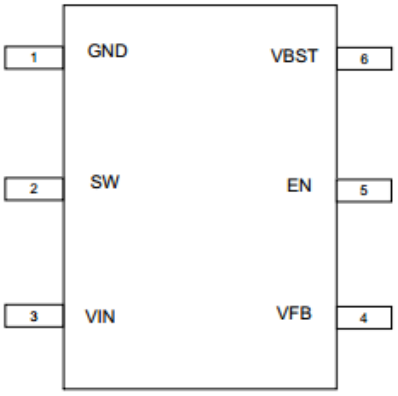


Figure 12: Pin Assignment

Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between VBST and SW pins.

Electrical Characteristics

T_J = -40°C to 150°C, VIN = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VIN)}$	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, V_{FB} = 0.8 V	TPS562200		230	330	µA
			TPS563200		190	290	
$I_{(VINSDN)}$	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V			3	10	µA
LOGIC THRESHOLD							
$V_{EN(H)}$	EN high-level input voltage	EN		1.6			V
$V_{FN(l)}$	EN low-level input voltage	EN				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
$V_{FB(TH)}$	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10mA, Eco-mode™ operation			772		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation		758	765	772	mV
$I_{(VFB)}$	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V	TPS562200		122		mΩ
			TPS563200		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C	TPS562200		72		mΩ
			TPS563200		39		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit (1)	DC current, V_{OUT} = 1.05 V, L_{OUT} = 2.2 µF	TPS562200	2.5	3.2	4.3	A
		DC current, V_{OUT} = 1.05 V, L_{OUT} = 1.5 µF	TPS563200	3.5	4.2	5.3	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature			155		°C
		Hysteresis			35		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{OVP}	Output OVP threshold	OVP Detect			125% x Vfbth		
V_{UVP}	Output Hiccup threshold	Hiccup detect			65% x Vfbth		
$t_{HiccupOn}$	Hiccup On Time	Relative to soft-start time			1		ms
$t_{HiccupOff}$	Hiccup Off Time	Relative to soft-start time			7		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage		3.45	3.75	4.05	V
		Hysteresis VIN voltage		0.13	0.32	0.55	

(1) Not production tested

E. MP8774GQ-Z 12A QFN16 (U154)

DESCRIPTION

The MP8774 is a fully integrated high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP8874 offers a very compact solution that achieves 12A of continuous output current with excellent load and line regulation over a wide input range. The MP8774 uses synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP8774 requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-16 (3mmx3mm) package.

FEATURES

- Output Adjustable from 0.6V
- Wide 3V to 18V Operating Input Range
- 12A Output Current
- 16mΩ/5.5mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 100μA Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Fixed 700kHz Switching Frequency
- External Programmable Soft Start-Up Time
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Security Cameras
- Portable Devices, XDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purpose

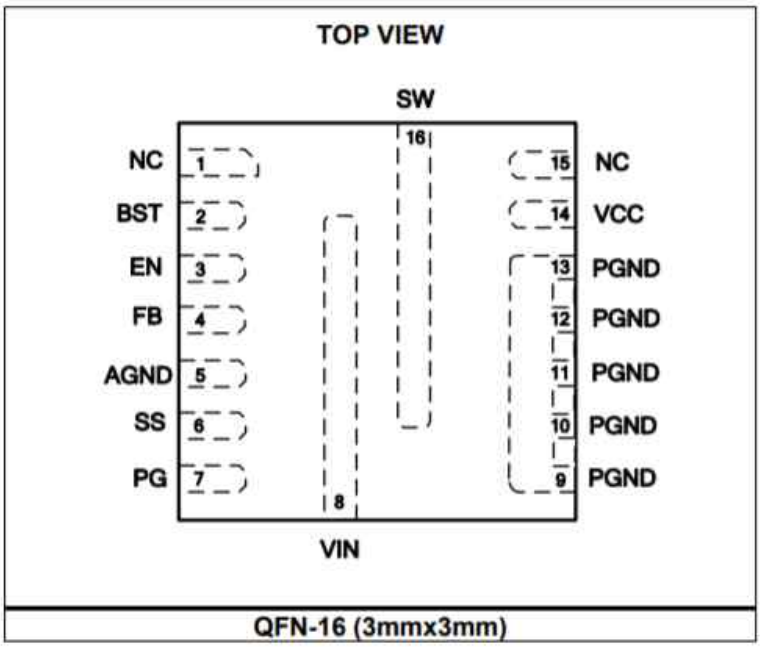
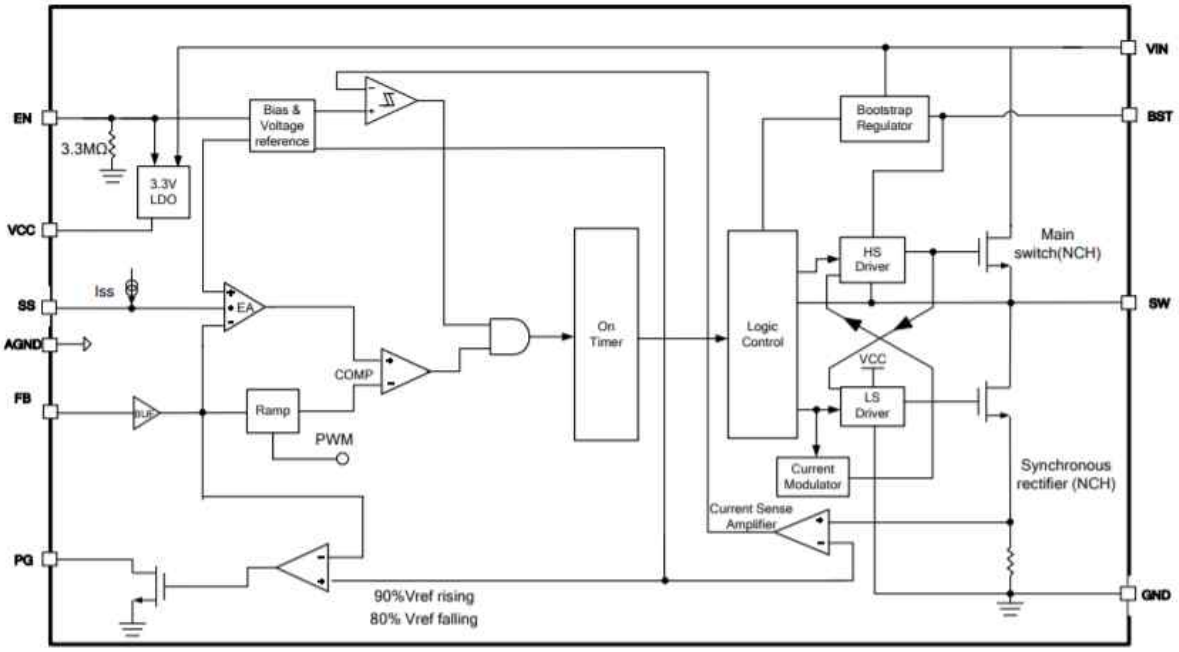


Figure 13: Pin Assignment

PIN FUNCTIONS

Package Pin #	Name	Description
1, 15	NC	**No connection.** NC must be left floating.
2	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. A BST resistor less than 4.7Ω is recommended.
3	EN	**Enable.** Pull EN high to enable the MP8774. When floating, EN is pulled down to GND and disabled by an internal 3.3MΩ resistor.
4	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider between output and GND.
5	AGND	**Signal ground.** AGND is not connected to the system ground internally. Ensure that AGND is connected to the system ground in the PCB layout.
6	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time to avoid inrush current at start-up.
7	PG	**Power good output.** The output of PG is an open drain. PG changes state if UVP, OCP, OTP, or OV occurs.
8	VIN	**Supply voltage.** The MP8774 operates from a 3 - 18V input rail. A capacitor (C1) is needed to decouple the input rail. Use a wide PCB trace to make the connection.
9 - 13	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during the PCB layout. PGND is recommended to be connected to GND with coppers and vias.
14	VCC	**Internal bias supply output.** Decouple VCC with a 1μF capacitor. Place the VCC capacitor close to VCC and GND.
16	SW	**Switch output.** Connect SW with a wide PCB trace.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		3		18	V
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			5	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	μA
MOSFET						
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		16		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 3.3V		5.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 17V, T_J = 25°C			1	μA
Current Limit and ZCD						
Valley current limit	I_{LIMIT_VY}		12	14		A
Short hiccup duty cycle (7)	D_{HICCUP}			10		%
ZCD	I_{ZCD}			200		mA
Switching Frequency and Minimum On/Off Timer						
Switching frequency	Fs		600	700	800	kHz
Minimum on time (7)	$T_{On\ MIN}$			50		ns
Minimum off time (7)	$T_{Off\ MIN}$			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	μA
Enable and UVLO						
EN rising threshold	$V_{EN\ RISING}$		1.1	1.25	1.4	V
EN falling threshold	$V_{EN\ FALLING}$		0.9	1	1.1	V
EN pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.6	2.8	3	V
VCC under-voltage lockout threshold	VCC_{HYS}			350		mV
VCC regulator	V_{CC}			3.4		V
VCC load regulation	Reg_{VCC}	I_{CC} = 5mA		3		%

ELECTRICAL CHARACTERISTICS (6) *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good UV rising threshold	$PGUV_{vth\_Hi}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{vth\_Lo}$		0.75	0.80	0.85	V_{FB}
Power good OV rising threshold	$PGOV_{vth\_Hi}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{vth\_Lo}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{Td}	Both edge		50		μs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	μA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD-HYS}			20		°C

NOTES:

6) Guaranteed by over-temperature correlation, not tested in production.

7) Guaranteed by design and characterization test.

F. LDO LM1117 (U130, U140)

Description

The LM1117 is a low power positive-voltage regulator designed to meet 1A output current and comply with SCSI-II specifications with a fixed output voltage of 2.85V. This device is an excellent choice for use in battery-powered applications, as active terminators for the SCSI bus, and portable computers. The LM1117 features very low quiescent current and very low dropout voltage of 700mV at a full load and lower as output current decreases. LM1117 is available as an adjustable or fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, and 5.0V output voltages. The LM1117 is offered in a 3-pin surface mount package SOT-223 & TO-263. The output capacitor of 10μF or larger is needed for output stability of LM1117 as required by most of the other regulator circuits.

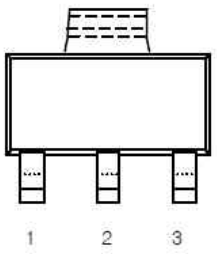
Features

- Output Current up to 1 A
- Low Dropout Voltage (700mV at 1A Output Current)
- Three Terminal Adjustable or Fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- 2.85V Device for SCSI-II Active Terminator
- 0.04% Line Regulaion, 0.1% Load Regulation
- Very Low Quiescent Current
- Internal Current andTerminal Limit
- Logic-Controlled Electronics Shutdown
- Surface Mount Package SOT-223 & TO-263 (D2-Pack)
- 100% Thermal Limit Burn-In

Application

- Active SCSI Terminators
- Portable/Plan Top/Notebook Computers
- High Efficiency Linear Regulators
- SMPS Post Regulators
- Mother B/D Clock Supplies
- Disk Drives
- Battery Chargers

SOT-223 PKG (FRONT VIEW)



PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin

ELECTRICAL CHARACTERISTICS FOR LM1117 S/T-AD(ADJUSTABLE)

(Refer to the test circuits, T_J=0 to 125℃ C_O=10㎌ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Reference Voltage	V_{REF}	$V_{IN}-V_O$ = 2V, I_O = 100mA, T_J = 25℃	1.238	1.25	1.262	V
Reference Voltage	V_{REF}	I_O = 10 to 1A, $V_{IN}-V_O$ = 1.4 to 10V	1.230		1.270	V
Line Regulation	ΔV_O	$V_{IN}-V_O$ = 1.5 to 13.75V, I_O = 10mA		0.035	0.2	%
Load Regulation	ΔV_O	$V_{IN}-V_O$ = 3V, I_O = 10mA to 1A		0.1	0.4	%
Temperature Stability	ΔV_O			0.5		%
Long Term Stability	ΔV_O	1000 hrs, T_J = 125℃		0.3		%
Operating Input Voltage	V_{IN}				7	V
Adjustment Pin Current	I_{ADJ}	$V_{IN} \leq$ 15V, I_{Load} =10mA		50	120	㎂
Adjustment Pin Current Change	ΔI_{ADJ}	$V_{IN}-V_O$ = 1.4 to 10V, I_O = 10mA to 1A		1	5	㎂
Minimum Load Current	$I_{O(MIN)}$	V_{IN} = 15V		1.7	5	mA
Output Current	I_O	$V_{IN}-V_O$ = 5V, T_J=25℃	800	950	1200	mA
Output Noise ($\%V_O$)	$_EN$	B = 10Hz to 10kHz, T_J = 25℃		0.003		%
Supply Voltage Rejection	SVR	I_O = 40mA , f = 120Hz, T_J = 25℃ $V_{IN}-V_O$ = 3V, V_{NIPPLE} = $1V_{PP}$	60	75		dB
Dropout Voltage	V_D	I_O = 100mA , V_{IN}=V_{OUT}+ 0.8V		1	1.1	V
		I_O = 500mA , V_{IN}=V_{OUT}+ 0.8V		1.00	1.15	V
		I_O = 1A , V_{IN}=V_{OUT}+ 0.8V		1.0	1.3	V
Thermal Regulation		T_A = 25℃ 30ms Pulse		0.003		%/W

ELECTRICAL CHARACTERISTICS FOR LM1117 S/T-1.5

(Refer to the test circuits, T_J=0 to 125℃ C_O=10㎌ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	V_{IN} = 4.5V, I_O = 10mA, T_J = 25℃	1.485	1.5	1.515	V
Output Voltage	V_O	I_O = 0 to 1A, V_{IN} = 3.9 to 10V	1.475		1.525	V
Line Regulation	ΔV_O	V_{IN} = 3.9 to 10V, I_O = 0mA		0.04	0.2	mV
Load Regulation	ΔV_O	V_{IN} = 3.9V, I_O = 0 to 1A		0.08	0.4	mV
Temperature Stability	ΔV_O			0.5		%
Long Term Stability	ΔV_O	1000 hrs, T_J = 125℃		0.3		%
Operating Input Voltage	V_{IN}	I_O = 100mA			7	V
Quiescent Current	I_D	$V_{IN} \leq$ 10V		5	10	mA
Output Current	I_O	V_{IN} = 7.5V, T_J = 25℃	800	950	1200	mA
Output Noise Voltage	$_EN$	B = 10Hz to 10kHz, T_J = 25℃		100		㎶
Supply Voltage Rejection	SVR	I_O = 40mA , f = 120Hz, T_J = 25℃ V_{IN} = 5.5V, V_{NIPPLE} = $1V_{PP}$	60	75		dB
Dropout Voltage	V_D	I_O = 100mA		1	1.1	V
		I_O = 500mA		1.05	1.15	V
		I_O = 800mA		1.1	1.2	V
Thermal Regulation		T_A = 25℃ 30ms Pulse		0.003		%/W

ELECTRICAL CHARACTERISTICS FOR LM1117 S/T-1.8

(Refer to the test circuits, T_J=0 to 125℃ C_O=10㎌ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_O	V_{IN} = 4.5V, I_O = 10mA, T_J = 25℃	1.782	1.8	1.818	V
Output Voltage	V_O	I_O = 0 to 1A, V_{IN} = 3.9 to 10V	1.772		1.828	V
Line Regulation	ΔV_O	V_{IN} = 3.9 to 10V, I_O = 0mA		0.04	0.2	mV
Load Regulation	ΔV_O	V_{IN} = 3.9V, I_O = 0 to 1A		0.08	0.4	mV
Temperature Stability	ΔV_O			0.5		%
Long Term Stability	ΔV_O	1000 hrs, T_J = 125℃		0.3		%
Operating Input Voltage	V_{IN}	I_O = 100mA			7	V
Quiescent Current	I_D	$V_{IN} \leq$ 10V		5	10	mA
Output Current	I_O	V_{IN} = 7.5V, T_J = 25℃	800	950	1200	mA
Output Noise Voltage	$_EN$	B = 10Hz to 10kHz, T_J = 25℃		100		㎶
Supply Voltage Rejection	SVR	I_O = 40mA , f = 120Hz, T_J = 25℃ V_{IN} = 5.5V, V_{NIPPLE} = $1V_{PP}$	60	75		dB
Dropout Voltage	V_D	I_O = 100mA		1	1.1	V
		I_O = 500mA		1.05	1.15	V
		I_O = 800mA		1.1	1.2	V
Thermal Regulation		T_A = 25℃ 30ms Pulse		0.003		%/W

6. MICROCONTROLLER APL5910

MTK G22 (U139)

The MSD95NTGW8J is MStar's advanced system-on-chip solution for flat panel integrated smart TV products. Building on the success of MStar's current solutions, the MSD95NTGW8J hosts the most advanced picture processing engine, MStarACE-PRO^{UC}, for all the *Experts* in various of TV video quality tuning fields to develop the state-of-the-art TV and DTV system.

MACE-PRO^{UC}, the Professional UC Edition of MStar video processor, includes all MStar's successful color-tuning tools and a newly added multi-dimensional color/sharpening/NR formula that can quickly reflect subtle or sudden changes in even darker, brighter, or mixture scenes. With this ultimate color processor, an specially designed color remapping system for modern wider gamut displays, and an easy-to-use color-tool UI, developers can quickly and easily identify PQ characteristic from the most high-end panel models to the most conventional panel models. The MStar innovated UltraClear DTV video processor adopts multi-frame video recovery technology to perfectly restore the contents/details, and eliminate the noise/artifacts from broadcasting or Internet videos.

The MSD95NTGW8J integrates DTV/multi-media all-purpose AV decoder, VIF demodulator, ATSC /ISDB-T/ DVB-C/ DVB-T/DVB-T2/DVB-S/DVB-S2/DVB-S2X demodulators, and Sound/Video processor into a single device. This allows the overall BOM to be significantly reduced and making the MSD95NTGW8J a very powerful smart TV solution.

The MSD95NTGW8J enables feature rich products that bring differentiation to the smart TV market. By the use of AV decoder which is capable of decoding a plethora of high definition content with Ethernet, USB connectivity and a powerful CPU, an MSD95NTGW8J based system can provide a high quality media-center experience.

The MSD95NTGW8J provides a legacy multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. Similarly the audio decoder is capable of decoding FM, AM, NICAM, A2, BTSC and sound standards.

The MSD95NTGW8J supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selection multiplexed for video and audio are integrated, including full SCART support with CVBS output.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MSD95NTGW8J has an ultra-low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

Features

MSD95NTGW8J is a Powerful ARM-based Smart TV solution that supports dual 8/10-bit LVDS output, channel decoding, MPEG decoding, 3D formatter, and media-center functionality enabled by a high performance AV CODEC and CPU

Key features includes,

1. *High performance Multi-core CPU and GPU*
2. *3D Formatter Engine*
3. *A Multi-Standard A/V Format Decoder*
4. *The MACE-PRO^{UC} Video Processor*
5. *Home Theater Sound Processor*
6. *Internet and Variety of Connectivity Support*
7. *Peripheral and Power Management*

- High Performance Micro-processor
  - ARM Advanced Multi-Core CPU
  - Maximum 64KB L1 cache
  - Maximum 512KB L2 cache
  - Neon supported
- 3D Graphic GPU
  - ARM Advanced Multi-Core GPU
  - Supports OpenGL ES 1.1/2.0
  - Supports OpenVG 1.1
- Transport Stream De-multiplexer
  - Supports one serial and two parallel TS interfaces, with or without sync signal
  - Maximum TS data rate is 140Mbit/s for serial and 56MByte/s for parallel
  - 128 general purpose PID filters and section filters for transport stream de-multiplexer
  - Supports time-shift function
  - Supports CSA v2, AES, 3DES/DES and Multi2 decrypted cipher engine
- HEVC/H.265 Video Decoder
  - Supports HEVC/H.265 video decoding.
  - Supports Main/Main-10 profile, level 5.1, high tier
  - Supports 8-bit/10-bit color depth
  - Supports resolution up to 4096x2160@60fps
  - Supports max bitrate upto 100 Mbps
- MPEG-2 Video Decoder
  - ISO/IEC 11172-2 MPEG-1 video format decoding
  - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
  - Supports resolution up to HDTV (1080p60, 1080i, 720p) and SDTV
  - Supports dual stream decoding for 3D content
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
  - Supports resolutions up to HDTV (1080p@60fps)
  - Supports FLV version1 video format decoding
  - Supports dual stream decoding for 3D content
- H.264 Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 5.2) video decoding
  - Supports resolution up to 4096x2160@60fps
  - Supports bitrate up to 135Mbps
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports SVAF 2ES (for Dual Decode)
  - Supports MVC 3D decoding upto 1080p@60fps
- VP8 Decoder Optional
  - Supports Google VP8 decoder
  - Supports resolution up to 1920x1080@30fps
  - Supports maximum bitrate upto 50Mbps
- VP9 Decoder Optional
  - Supports Google VP9 decoder
  - Supports 4:2:0 subsampling and 8bit/10bit color depth
  - Supports max resolution and frame rate 4096x2160@60fps
  - Supports max birate upto 100Mbps

- AVS+ Decoder Optional
  - Supports Broadcasting profile, level 6.0.1.08.60 (AVS+)
  - Supports Jizhun profile, level 6.0
  - Supports bitrate up to 50Mbps
  - Supports resolution up to 1920x1080@60fps
  - Supports dual stream decoding
- RealMedia Decoder Optional
  - Supports RV8, RV9, RV10 decoders
  - Supports file formats with RM and RMVB
  - Supports maximum resolution up to 1080p@30fps
  - Supports Picture Re-sampling
  - Supports in-loop de-block for B-frame
- Hardware PNG / GIF Decoder
  - Supports up to 8192 x 8192 (per channel 8 bits), or 4096 x 8192(per channel 16 bits) pixel image
  - PNG format 1bpp/2bpp/4bpp/8bpp index(palette) mode support
  - PNG transparency mode support
  - Interlaced / non-interlaced GIF support
  - ARGB8888, RGB565, YUV422(YUYV),YUV422(YVYU),gray, gray with alpha output format support
- Hardware JPEG Decoder
  - Supports upto 1280x720@30fps
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
  - Supports both color and grayscale pictures
  - Supports sequential mode, single scan
  - Supports programmable Region of Interest (ROI)
  - Following the file header scan the hardware decoder fully handles the decode process
- VC-1 Video Decoder Optional
  - Supports SMPTE-421M (VC1 video) decoding up to AP@L3 (2048x1024p60)
  - Supports dual stream decoding for 3D content
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Supports configurable CVBS or Y/C S-video inputs
  - Supports Teletext, Closed Caption (analog CC 608/ analog CC 708) and V-chip
- Multi-Standard TV Sound Processor
  - Supports BTSC/A2 demodulation
  - Supports NICAM/FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC mode
  - Supports Mono/Stereo/Dual in A2/NICAM mode
  - Built-in audio sampling rate conversion (SRC)
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
  - Advanced sound processing options available, for example: Dolby(1), DTS(2), DBX-TV(3)
  - Supports digital audio format decoding: MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3) Optional, Dolby Digital Plus Optional, AAC-LC, HE-AAC, WMA and WMA9 Pro
  - Supports Multi-stream programs :
  - MS11 Optional, MS12 v1.3 (Profile B) Optional, MS12 v2.2 (Dolby Atmos) Optional and DTS M6 Optional
  - Dolby Digital Encoder for trans-coding streams to Dolby Digital 5.1 (DDCO) , DTS M6 multi-stream decoder/encoder
  - Supports Audio Description
  - Supports MPEG audio encoding
  - Supports time-shifting PVR
  - Supports programmable delay for audio/video synchronization

- Audio Interface
  - Two L/R audio line-inputs
  - One L/R outputs for main speakers and additional line-outputs
  - Supports stereo headphone driver
  - I2S digital audio output
  - S/PDIF digital audio output
  - Supports HDMI receiver ARC function
  - Support PDM input for 2~8 channels digital microphone
- Analog RGB Compliant Input Ports
  - Two analog ports support up to 1080P
  - Supports PC RGB input up to SXGA@75Hz
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and Sync-on-Green
  - Automatic color calibration
- Analog RGB Auto-Configuration & Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain
  - Sync Detection for H/V Sync
- DVI/HDCP/HDMI Compliant Input Ports
  - Four HDMI/DVI Input ports
  - HDMI 2.0b/1.4b Compliant
  - MStar iSwitch for fast HDMI switching
  - HDCP 2.2/1.4 Compliant
  - Supports HDMI CEC
  - Supports HDMI 3D formats
  - Supports HDMI ARC
  - Robust receiver with excellent long-cable support
- MStar High Performance Video Processor
  - Video Processing Engine
    - Supports up to 4K UHD@60p
    - 10-/12-bit Internal Data Processing
    - Dual-Engine Architecture supporting PIP/PBP
    - Arbitrary Frame Rate Conversion
  - Video Care Technology
    - Video Line Broken Artifact Detection and Removal
    - Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
  - Fully Programmable multi-function scaling engine
    - High-Tap Filters with Programmable Parameter
    - An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
    - Nonlinear Video Scaling supports various modes including Panorama
    - Supports Dynamic Scaling for RM, VC-1 **Optional**
    - Fully Programmable Zoom Ratios for Up/Down Scaling
    - Independent Horizontal and Vertical Zoom
  - Deinterlacer
    - Motion Compensated Video Deinterlacing with Motion Object Stabilizer
    - Motion Adaptive Deinterlacer
    - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
    - Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
  - MStar Genuine 3D
    - Supports Mandatory 3D Format
  - Motion Frame Rate Conversion
    - Supports Frame Repeat Frame Rate Conversion
  - Backlight Technology
    - Supports Direct and Edge Types Local Dimming
    - Programmable Light Spread Profile
    - Content Adaptive LCD Backlight Control
  - High Dynamic Range
    - Supports SMPTE ST-2084 / ST-2086
    - Supports ARIB STD-B67 (Hybrid Log Gamma) / BT.2100
    - Supports 2094-40 (HDR10 plus)
    - Ultra HD Premium Ready
    - Dolby Vision **Optional**
  - Response Time Compensation
    - Supports Overdrive Technology

- MStar Professional PQ Engine
  - UltraClear
    - MPEG Artifact Removal
      - Advanced Adaptive Block Noise Reduction
      - Advanced Mosquito Noise Cancellation
    - UltraClear Noise Reduction
      - 3D Motion-Estimation Temporal Filtering
    - 3D Noise Reduction
      - 3D Temporal Noise Reduction for Lousy Air/Cable Input
  - S-Powers
    - Video Enhancement Processor
      - Advanced 3D Independent Multi-Band Control Sharpness Technology
      - Advanced Video Enhancement Algorithm provides Aliasing/Ringing Suppression
      - Advanced Chroma Transient Improvement
      - Supports Luma Transient Improvement
    - Super Resolution
      - Local Detail Enhancement
      - SuperiorClear Multi-Directional Jagged Compensation Technology
  - MACE
    - MStar Advanced Color Engine
      - MStar Graffito Color Manager
      - Color Stain Removal Technology
    - Standard Color Format and Processing
      - Fully programmable Input/Ouput CSC
      - BT601, BT709, BT2020(CL/NCL)
      - xvYCC601, xvYCC709
      - AdobeRGB, AdobeYCC601
      - sRGB, sYCC601
      - Fully Programmable 12-bits RGB Gamma
    - Gamut Mapping
      - Nonlinear/Linear RGB Domain Gamut Mapping
      - Supports 2D Gamut Mapping
      - Supports 3D Gamut Mapping Engine
  - Luce
    - Contrast Enhancement
      - Real-Time, Content Adaptive Contrast Enhancement with Chroma Compensated
      - Ultra-Contrast Dimming
    - SDR to HDR
      - MaxVivid
- Output Interface
  - Single/Dual link 8/10-bit LVDS output
  - Supports panel resolution up to Full HD 1920x1080@ 60Hz (LVDS 2-ch)
  - 8-lane 8/10-bit Vby1 output (configurable width: 2/4/8 lanes)
  - Supports panel resolution up to Ultra HD @ 60Hz (Vby1 8 lanes)
  - Supports OSD bypass to MStar FRC 120Hz/240Hz chip (optional)
  - Supports programmable timing controller
  - Supports mini-LVDS 2-ch interface, panel resolution up to Full HD @ 60Hz
  - Supports TTL output, update to 1920x1080@ 60Hz
  - Supports EPI interface, panel resolution up to Full HD @ 60Hz
  - Supports USI-T interface, panel resolution up to Ultra HD @ 60Hz
  - Supports iSP interface, panel resolution up to Ultra HD @ 60Hz
  - Supports CEDS interface, panel resolution up to Ultra HD @ 60Hz
  - Supports CMPI interface, panel resolution up to Ultra HD @ 60Hz
  - Supports CHPI interface, panel resolution up to Ultra HD @ 60Hz
  - Supports CSPI interface, panel resolution up to Ultra HD @ 60Hz
  - Supports dithering options
  - Spread spectrum output frequency for EMI suppression

- Supports 60Hz 3D polarized panel (line interleave)
- Supports Cinema output mode

- CVBS Video Output
  - Supports CVBS online bypass output
- 2D Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill and text draw
  - Supports BitBlt, stretch BitBlt, italic Bitblt, Mirror BitBlt and rotate BitBlt
  - Supports alpha-blending operation
  - Supports source/destination color key and alpha key
  - Supports dither
  - Supports color space conversion and format transformation
  - Raster Operation (ROP)
  - Supports DFB and Porter-Duff operation
- VIF Demodulator
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
  - Supports low IF architecture
  - Audio/Video internal dual-path processor
  - Locking range improvement
- ATSC Demodulator
  - ATSC A/53 compliant 8VSB
  - ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
  - 2010 - A74 compliant
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - Integrated deinterleaver
    RAM for Level 1 J =1 and Level 2 J= 1,2,3.4
  - Supports LIF interfaces
- ISDB-T Demodulator
  - Compliant with ISDB-T ARIB STD-B31
  - Compliant with ISDB-Tsb ARIB STD-B29
  - Supports all modes defined in ISDB-T spec
  - Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
  - Support LIF interfaces
  - Impulse-noise suppression
  - Phase noise compensation
  - Outside-GI performance improvement
  - CNR performance improvement
- DVB-C Demodulator
  - Compliant with ITU J.83 Annex A/C DVB-C (EN 300 429)
  - Supports 1-7.2 M Baud symbol rate
  - Automatic blind channel scan (constellation and symbol rate)
  - Supports LIF interfaces
  - IIS performance improvement
- DVB-T Demodulator
  - Compliant with DVB-T (ETSI EN 300 744)
  - Nordig 2.2.2, D-book 7.0 compliant
  - Accepts low IF inputs in 6, 7, 8MHz channel bandwidths
  - Supports all guard intervals (1/32 to 1/4)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM)
  - Ultra fast automatic blind UHF/VHF channel scan
  - Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
  - Phase-Noise suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - CNR performance improvement
  - Outside-GI performance improvement
- DVB-T2 Demodulator
  - Compliant with DVB-T2 (ETSI EN 302 755) v1.3.1, T2-base & T2-Lite profile
  - Nordig Unified 2.2.2, D-Book 7.0 compliant
  - Supports all guard intervals (1/128 to 1/4)
  - Supports all FFT modes from 1K to 32K

- Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
- Supports all constellations (QPSK, 16-QAM, 64-QAM, 256-QAM)
- Transmit diversity (MISO) support
- Supports all scattered pilot patterns (PP1 to PP8)
- Supports rotated and non-rotated constellations
- Supports single and multiple PLPs
- Accept low IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Outside GI improvement
- Locking time improvement

■ DVB-S Demodulator
- Compliant with DVB-S (ETSI EN 300 421)
- Data Rate: 1-70 Msps
- Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors
- Improved CNR performance

■ DVB-S2 Demodulator
- Compliant with DVB-S2 (ETSI EN 302 307)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 16APSK, 1-57 Msps for 32APSK
- Constellations: QPSK , 8PSK , 16APSK and 32APSK
- QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
- 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10
- 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
- 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10
- Support CCM and VCM
- Support Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

■ DVB-S2X Demodulator
- Compliant with DVB-S2 Extensions (ETSI EN 302 307-2, Broadcast services except for Channel Bonding)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 8APSK-L, 16APSK, 16APSK-L, 1-57 Msps for 32APSK, and 32APSK-L
- Constellations: QPSK , 8PSK, 8APSK-L, 16APSK, 16APSK-L, 32APSK, and 32APSK-L
- QPSK Code Rates: 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 13/45, 9/20, 11/20
- 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10, 23/36, 25/36, 13/18
- 8APSK-L Code Rates: 5/9, 26/45
- 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 26/45, 3/5, 28/45, 23/36, 25/36, 13/18, 7/9, 77/90
- 16APSK-L Code Rates: 5/9, 8/15, 1/2, 3/5, 2/3
- 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10,

32/45, 11/15, 7/9
- 32APSK-L Code Rates: 2/3
- Support CCM and VCM
- Support Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.05, 0.1, 0.15, 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

■ Connectivity
- USB 2.0 host ports x 3 + (host + device) x 1
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Built-in 10/100Mbps Ethernet PHY interface
- Supports Ethernet Wake-On-Lan

■ Miscellaneous
- DRAM interface supporting 64-bit DDR3 or DDR4
- Supports PVR
- Flash interface for external eMMC support
- Power control module with ultra-low power MCU available in standby mode
- 758-ball BGA package
- Operating Voltages: Core Power, 1.5V (DDR3), 1.22V (DDR4) and 3.3V (I/O and analog)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14	3.3	3.46	V
1.5V Supply Voltages (DDR3)	V_{VDD_15}	1.43	1.5	1.57	V
1.22V Supply Voltages (DDR4)	V_{VDD_122}	1.19	1.22	1.25	V
2.5V Supply Voltages (DDR4)	V_{VDD_25}	2.38	2.5	2.62	V
Core Supply Voltages	V_{VDD_core}		TBD		V
CPU Supply Voltages	V_{VDD_cpu}		TBD		V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Table 4: Recommended operating condition

7. 1.5GB DDR3 SDRAM NANYA NT5CB128M16JR-FL 2133 (U3)

NANYA 128MX16 NT5CB128M16JR-FL 2133 (U110-U113)

Description

Basic Functionality

The DDR3(L) SDRAM is a high-speed dynamic random access memory internally configured as an eight-bank DRAM. The DDR3(L) SDRAM uses an 8n prefetch architecture to achieve high speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3(L) SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3(L) SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A14 select the row). The address bit registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3(L) SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

Features

- **JEDEC DDR3 Compliant**
  - 8n Prefetch Architecture
  - Differential Clock(CK/$\overline{CK}$) and Data Strobe(DQS/$\overline{DQS}$)
  - Double-data rate on DQs, DQS and DM
- **Data Integrity**
  - Auto Self Refresh (ASR) by DRAM built-in TS
  - Auto Refresh and Self Refresh Modes
- **Power Saving Mode**
  - Power Down Mode
- **Signal Integrity**
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 ohm ± 1%)
- **Signal Synchronization**
  - Write Leveling via MR settings [5]
  - Read Leveling via MPR
- **Interface and Power Supply**
  - SSTL_15 for DDR3:VDD/VDDQ=1.5V(±0.075V)
  - SSTL_135[3] for DDR3L:VDD/VDDQ=1.35V(-0.067/+0.1V)

AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter		Rating			Unit	Note
			Min.	Typ.	Max.		
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6,7
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6,7

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. Maximun DC value may not be great than 1.425V.The DC value is the linear average of VDD/ VDDQ(t) over a very long period of time (e.g., 1 sec).
4. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
5. Under these supply voltages, the device operates to this DDR3L specification.
6. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation.
7. 1.35V DDR3L are backward compatible to 1.5V DDR3 parts.

8. 8 GB EMMC MT29F4G08ABAEAWP (U133)

SAMSUNG EMMC 8GB KLM8G1GETF-B041 BGA153 (U128)FEATURES

Description

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a sim-ple read and write to memory using MMC protocol v5.1 which is a industry standard. eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance. There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market. The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

Key Features

- Embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard

  - Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types

  - Non-supported Features : Large Sector Size (4KB)
- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz

  MMC I/F Boot Frequency : 0 ~ 52MHz
- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power →VCCQ(1.70V ~ 1.95V), Memory power → VCC(2.7V ~ 3.6V)

Item	Min	Max	Unit
V_{CCQ}	1.70	1.95	V
V_{CC}	2.7	3.6	V
V_{SS}	-0.5	0.5	V

Table 5: Supply Voltage

9. USB INTERFACE

USB POWER SWITCH ADJ SAFE TPS25221 SOT23-6 (U117-U109)

1 Features

- 2.5-V to 5.5-V $V_{OPERATING}$
- Pin-to-Pin with TI Switch Portfolio
- 2-A I_{CONT_MAX}
- 0.277-A to 2.7-A Adjustable I_{LIMIT} (±10% at 2.7 A)
- 70-mΩ (typical) R_{ON}
- 2-µs Short Circuit Response
- 8-ms Fault Reporting Deglitch
- Reverse Current Blocking (when disabled)
- Built-In Soft Start
- UL 60950 and UL 62368 Recognition Pending
- 15-kV ESD Protection per IEC 61000-4-2 (with external capacitance)

2 Applications

- USB Ports/Hubs, Laptops, Desktops
- High-Definition Digital TVs
- Set Top Boxes
- Optical Socket Protection

3 Description

The TPS25221 is intended for applications such as USB where heavy capacitive loads and short circuits may be encountered. The programmable current-limit threshold maybe set between 277 mA and 2.7 A (typical) using an external resistor. Current-limit accuracy as tight as ±10% can be achieved at the higher current-limit settings. The power-switch rise and fall times are controlled to minimize current surges during turn on and turn off.

The TPS25221 limits output current to the programmed level when the output load attempts to exceeds the current-limit threshold. The $\overline{FAULT}$ output asserts low during overcurrent conditions.

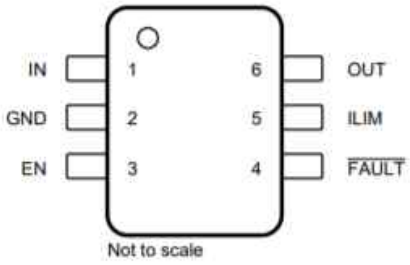
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25221	SOT-23 (6)	2.90 mm x 1.60 mm
	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

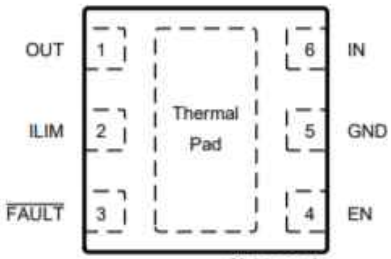
Pin Configuration and Functions

DBV PACKAGE
SOT-23 6-Pin
Top View



Not to scale

DRV PACKAGE
WSON 6-Pin
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	WSON		
IN	1	6	I	Input voltage and power switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to IC
GND	2	5	--	Ground connection
EN	3	4	I	Enable input, logic high/low turns on power switch
$\overline{\text{FAULT}}$	4	3	O	Active-low open-drain output, asserted during over-current, or over-temperature conditions
ILIM	5	2	O	External resistor used to set current limit threshold
OUT	6	1	O	Power switch output, connect to load
Thermal Pad	--	PAD	--	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect thermal pad to GND pin externally.

7.5 Electrical Characteristics

over recommended operating conditions, $V_{EN} = V_{IN}$, R_{FAULT} = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance	DBV package, T_J = 25°C			70	80	mΩ
		DBV package, –40°C ≤T_J ≤125°C				110	
		DRV package, T_J = 25°C			70	92	
		DRV package, –40°C ≤T_J ≤125°C				122	
t_r	Rise time, output	V_{IN} = 5.5 V	C_L = 1 µF, R_L = 100 Ω, (see 図 1)		0.55	0.95	ms
		V_{IN} = 2.5 V			0.35	0.62	
t_f	Fall time, output	V_{IN} = 5.5 V			0.24	0.3	
		V_{IN} = 2.5 V			0.22	0.28	
ENABLE INPUT EN OR $\overline{EN}$							
	Enable pin turn on/off threshold			0.8		1.6	V
I_{EN}	Input current	V_{EN} = 0 V or 5.5 V		-0.5	0	0.5	µA
t_{on}	Turnon time	C_L = 1 µF, R_L = 100 Ω, (see 図 2)				3	ms
t_{off}	Turnoff time	C_L = 1 µF, R_L = 100 Ω, (see 図 2)				0.7	ms
CURRENT LIMIT							
I_{OS}	Current-limit threshold (Maximum DC output current I_{OUT} delivered to load) and Short-circuit current, OUT connected to GND	R_{ILIM} = 20 kΩ	T_J = 25°C	2585	2720	2850	mA
			–40°C ≤T_J ≤125°C	2560		2880	
		R_{ILIM} = 30 kΩ	T_J = 25°C	1710	1820	1930	
			–40°C ≤T_J ≤125°C	1700		1945	
		R_{ILIM} = 80 kΩ	T_J = 25°C	630	690	755	
			–40°C ≤T_J ≤125°C	610		790	
		R_{ILIM} = 210 kΩ	T_J = 25°C	220	275	330	
			–40°C ≤T_J ≤125°C	210		370	
t_{IOS}	Response time to short circuit	V_{IN} = 5 V (see 図 4)			1.5		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disable	V_{IN} = 5.5 V, No load on OUT, V_{EN} = 0 V,R_{ILIM} = 20 kΩ			0.02	0.5	µA
I_{SE}	Supply current, switch enable	V_{IN} = 5.5 V, No load on OUT ,R_{ILIM} = 20 kΩ			75	90	µA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising			2.37	2.47	V
	Hysteresis, IN	T_J = 25 °C			45		mV
$\overline{FAULT}$ FLAG							
V_{OL}	Output low voltage, $\overline{FAULT}$	$I_{\overline{FAULT}}$ = 1 mA				180	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 5.5 V				0.5	µA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or de-assertion due to overcurrent condition		6	8	12	ms
THERMAL SHUTDOWN							
	Thermal shutdown threshold				165		°C
	Thermal shutdown threshold in current-limit				145		°C
	Hysteresis				20		°C

10. CI INTERFACE

17MB170 Digital CI ve Smart Card Interface Block diagram:

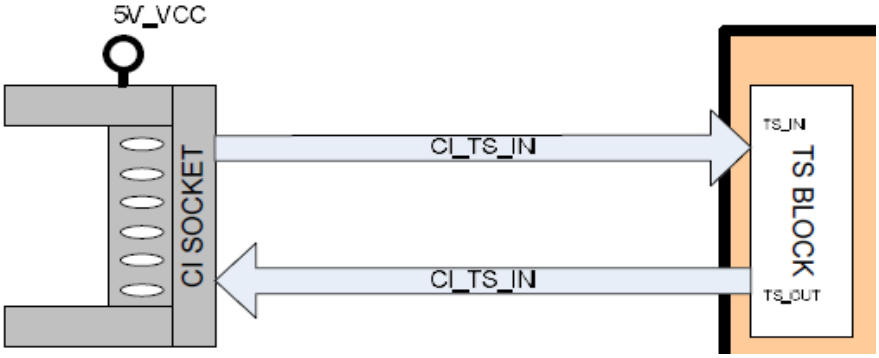


Figure 14: CI interface

11. SOFTWARE UPDATE

MAIN SOFTWARE UPDATE

In MB170 project, please follow software update procedure:

Method-1

1. Copy MstarUpgrade.bin to USB stick (root directory, FAT32)
2. Enter M-Boot console first (Long press "ENTER" key on Tera Term Console when your device reboot then do AC On)
3. Plug the USB stick to your target board
4. Execute "custar" in M-Boot console to perform upgrading

Method-2

1. Copy upgrade_loader.pkg to root folder of USB stick (or copy upgrade_loader_no_tvcertificate.pkg if you don't want to erase keys, credentials, etc.)
2. Insert USB disk to one of the USB ports on your TV
3. Power on TV and wait until you see the bootlogo
4. You should see logs like below

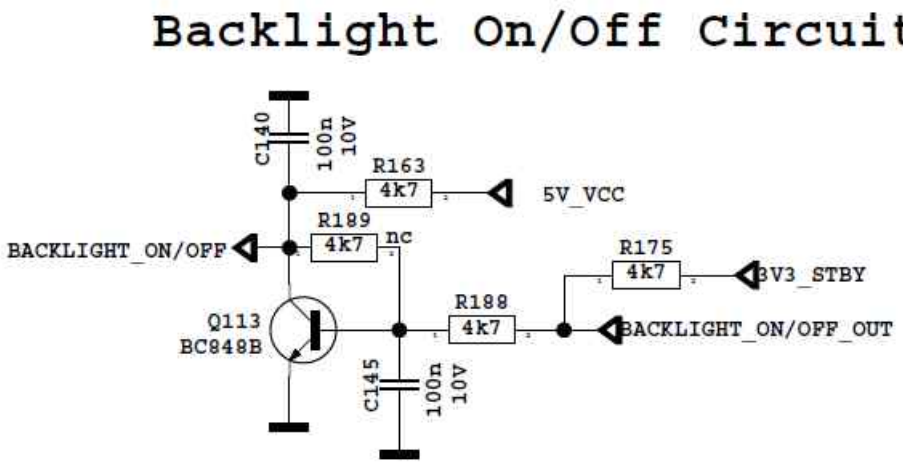
12. TROUBLESHOOTING

A. NO BACKLIGHT PROBLEM

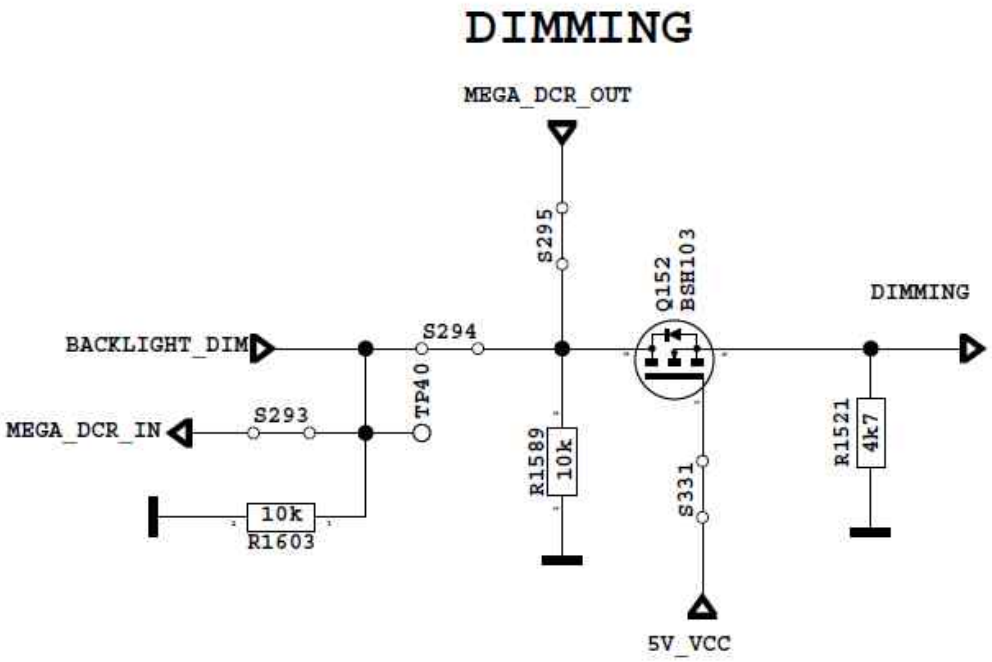
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

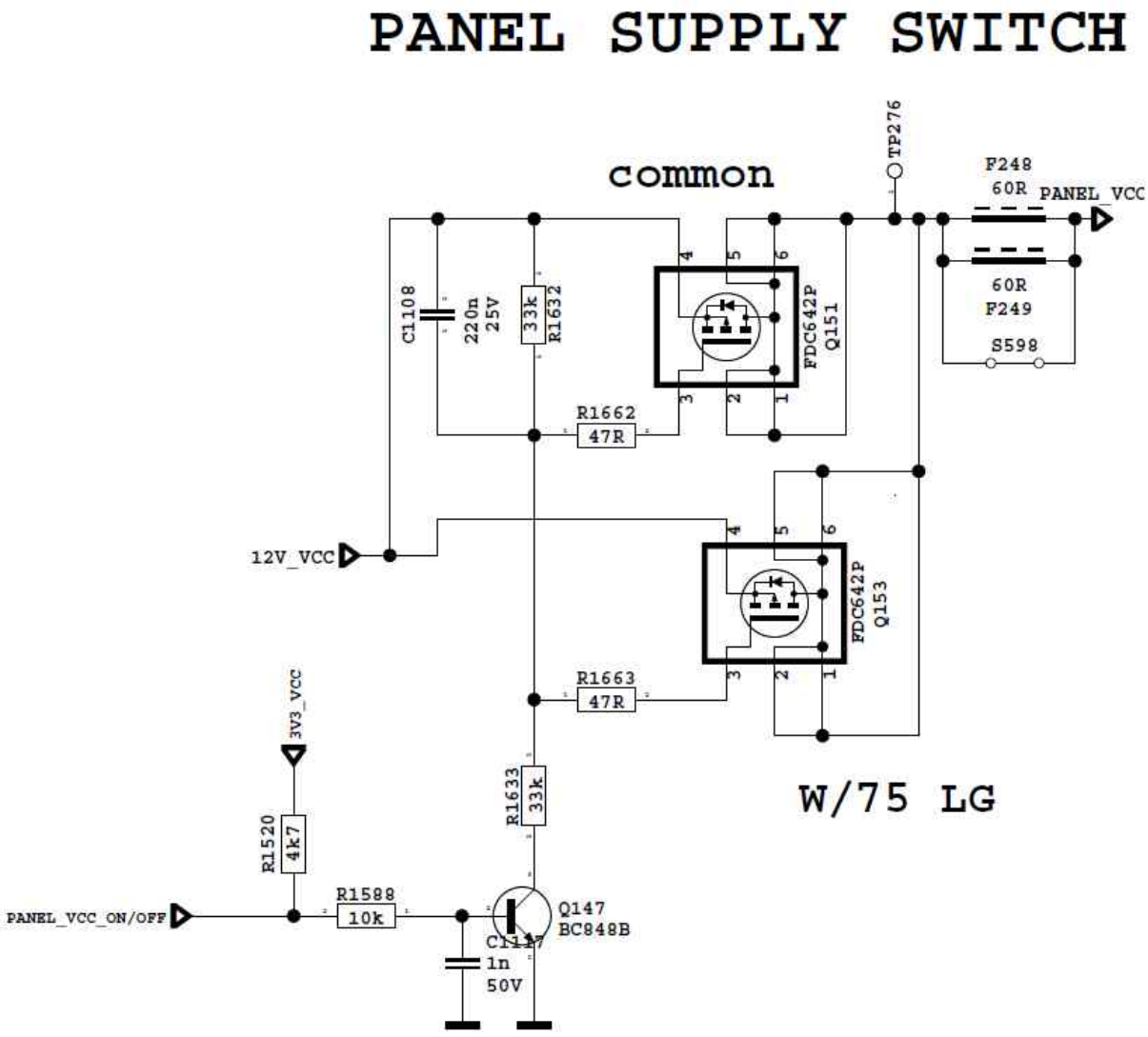
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q113 must be low when the backlight is OFF. If it is a problem, please check Q181. Also it can be tested in TP500 or Pin5 of CN2 in main board. Please also check panel cables.



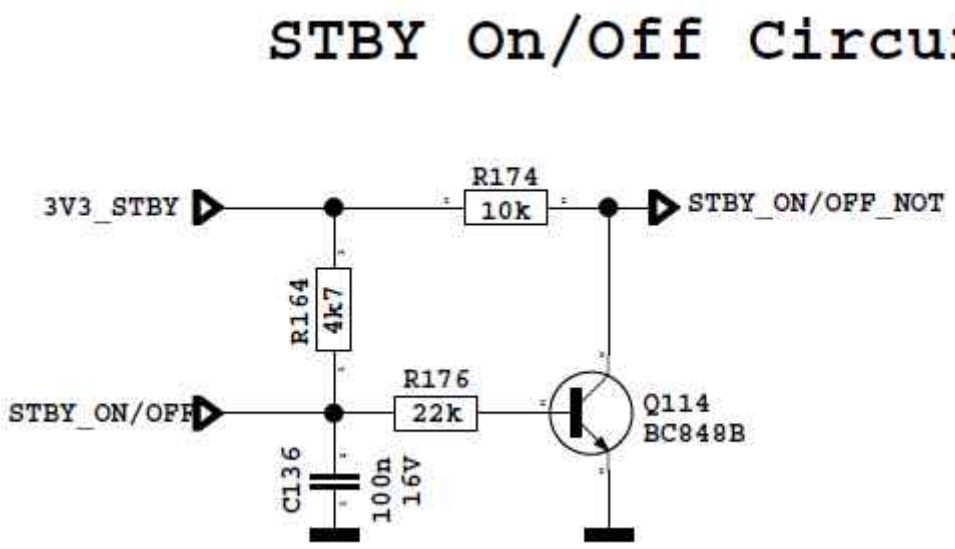
Dimming pin should be high or square wave in open position. If it is low, please check S294 for MTK side. It also can be checked at TP499. Please also check panel or power cables and connectors.



Panel power supply should be in panel specs. Please check Q151, shown below; also it can be checked TP276.



STBY_ON/OFF should be low for TV on condition, please check Q114's collector.

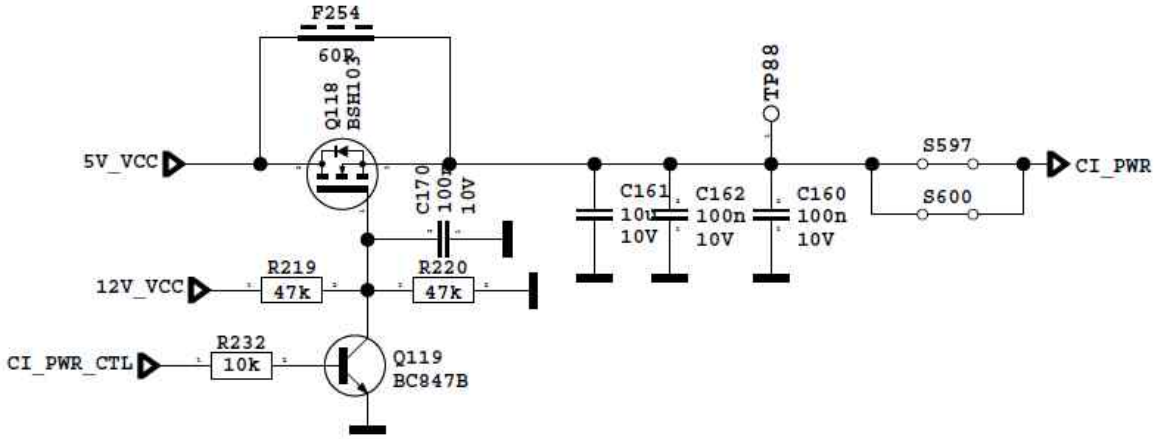


B. CI MODULE PROBLEM

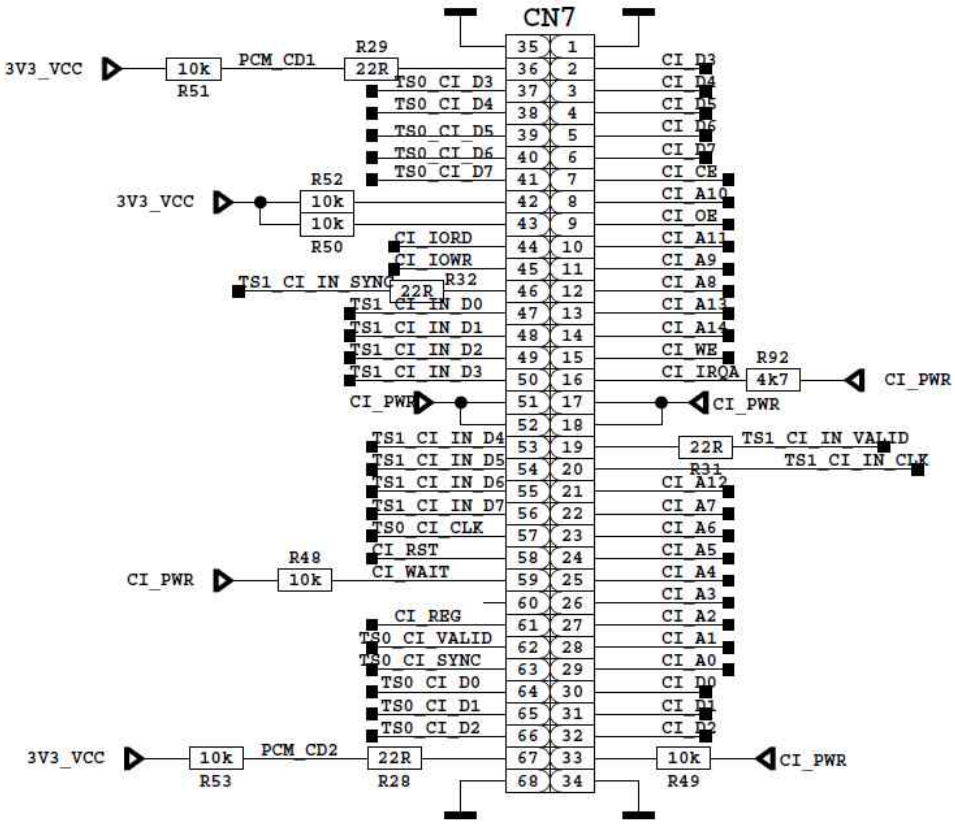
Problem: CI is not working when CI module inserted.

Possible causes: Supply, supply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.



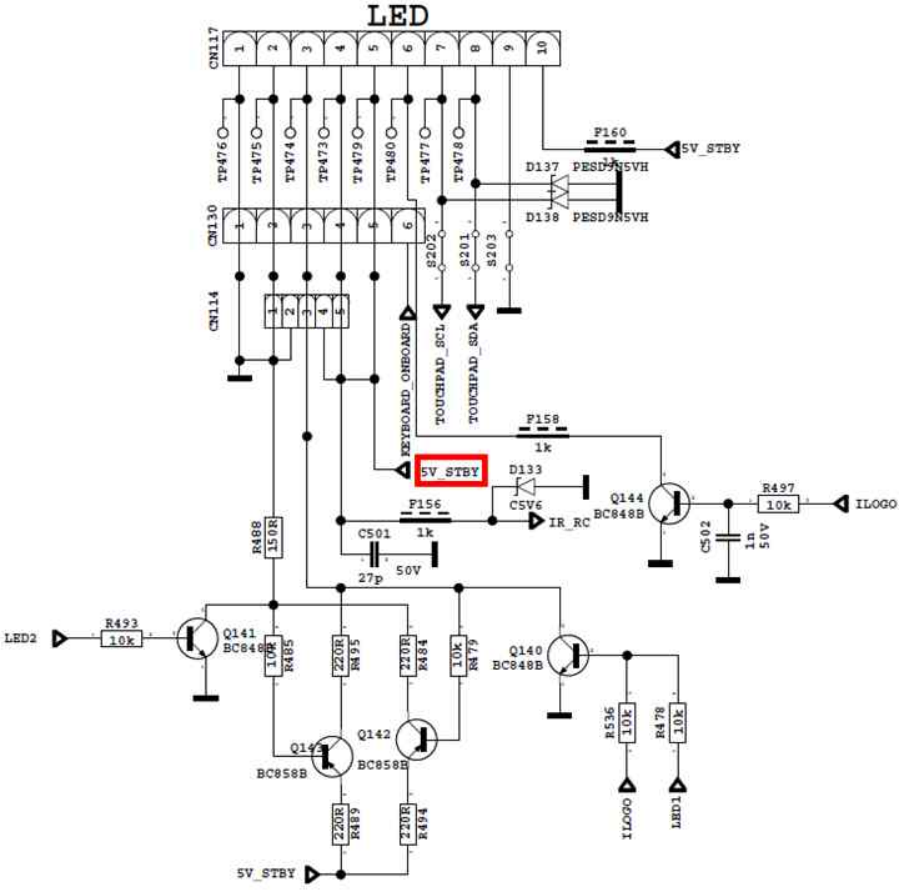
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.



C. IR PROBLEM

Problem: LED or IR not working

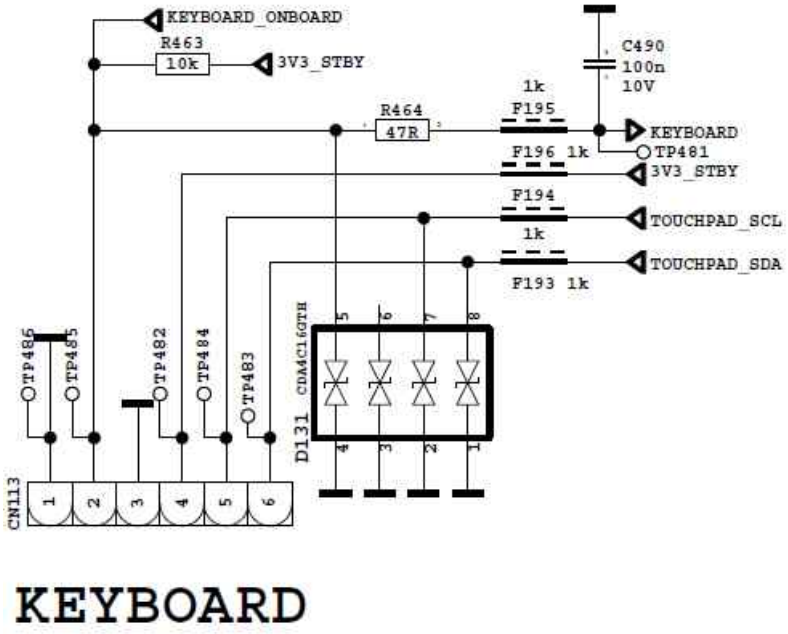
Check LED card supply on MB170 chasis.



D. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on MB170.

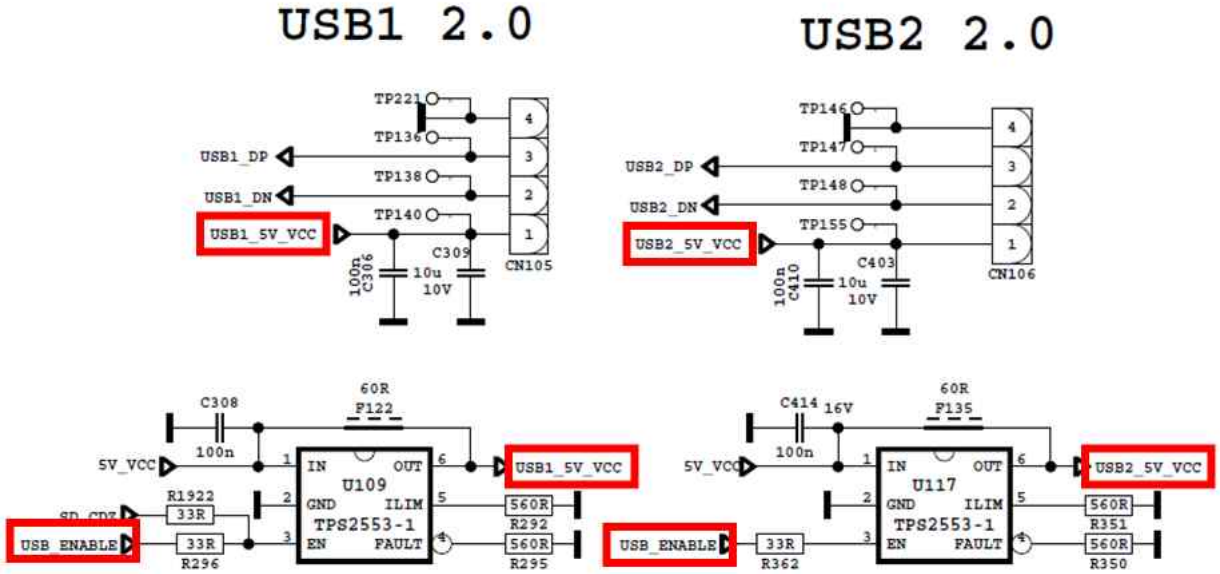


E. USB PROBLEMS

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

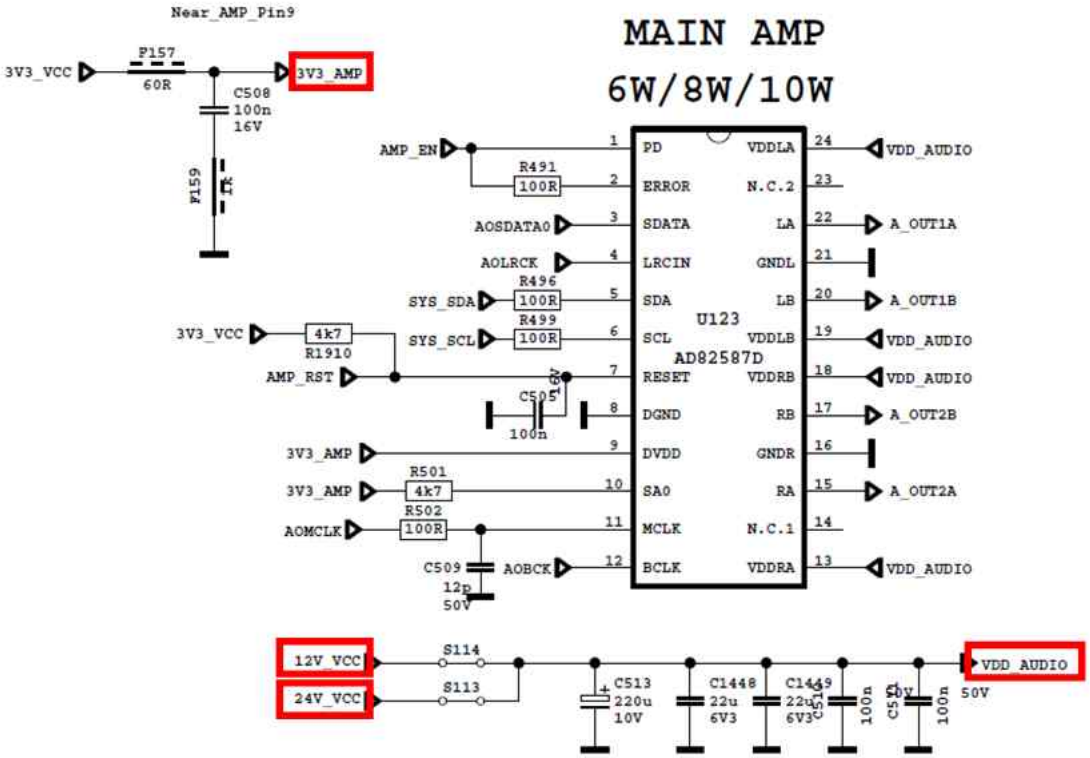
USB Control is optional, so U109 and U117 may not be added. Check supply voltages only.

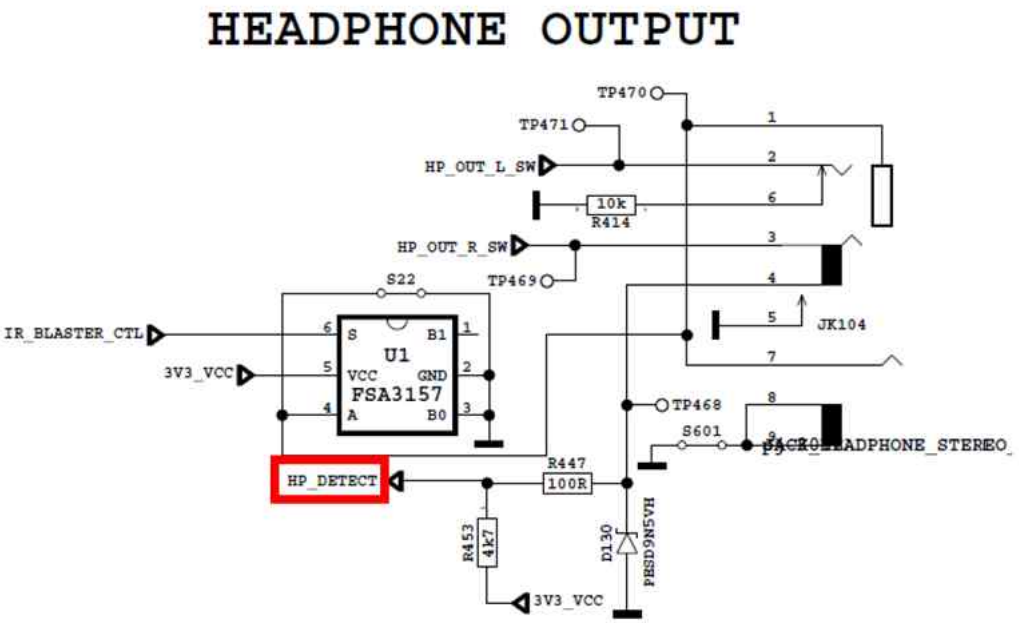


F. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 24V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3V.





G. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm program. These printouts may give a clue about the problem. You can use VGA for Teraterm program connection.

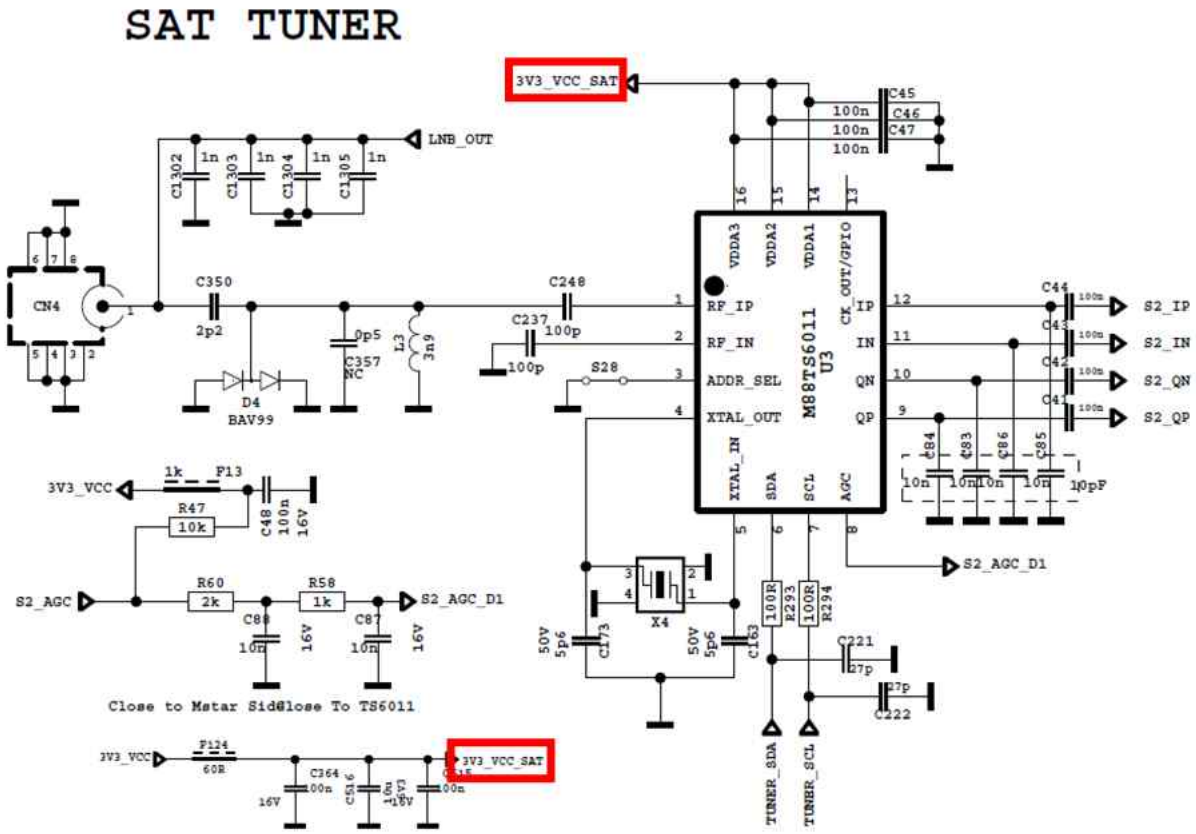
H. NO SIGNAL PROBLEM IN DVB-S/S2 MODE

Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check M88TS6011 (U3) supply voltages; 3V3_VCC_SAT.

If the above measurements are OK, then measure the voltage from the PIN1 of U3.

If the PIN9 voltage is equal to 0V, please check i2c waveforms and software. If the PIN9 voltage is lower than 1V(e.g: 0.8Vor 0.3V), change the U3 with a new part.

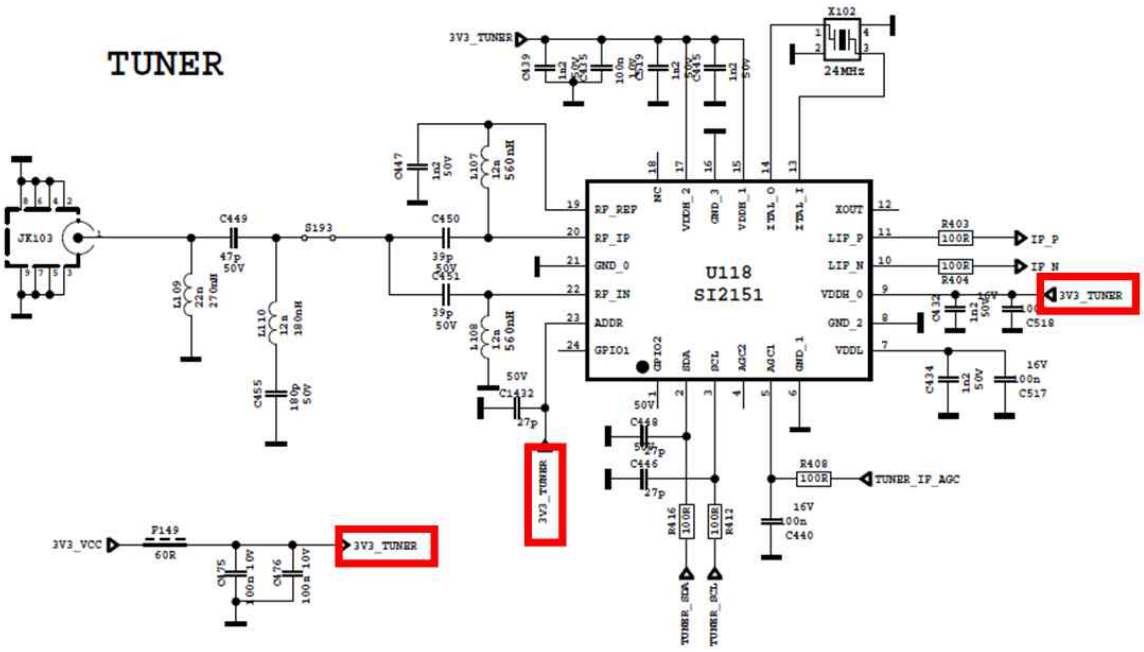


İ. NO SIGNAL PROBLEM IN DVB-T MODE

Problem: No signal or Low signal in DVB-T mode.

Check signal cables and LNB voltage, if there is no problem, check SI2151 (U118) supply voltages; 3V3_TUNER.

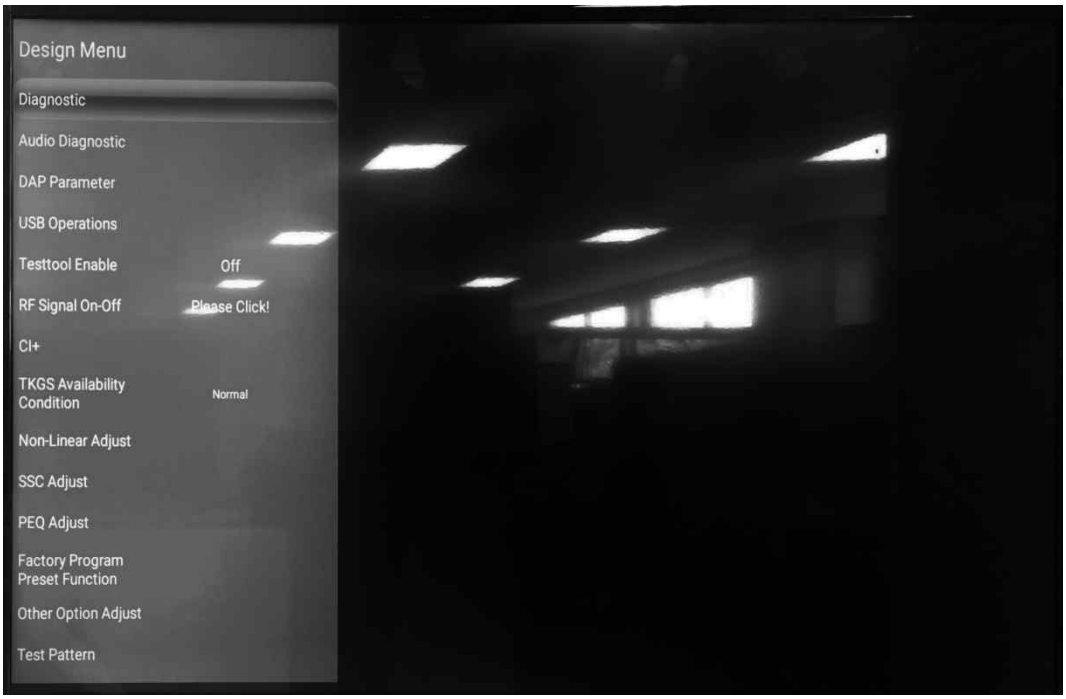
If the above measurements are OK, then change the U118 with a new part.



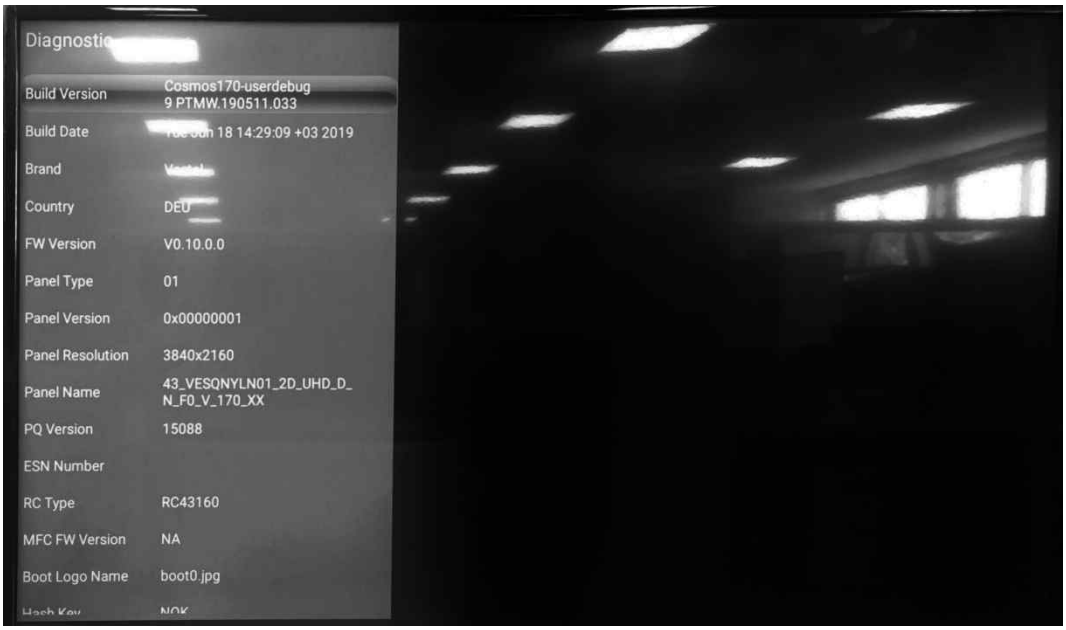
13. SERVICE MENU SETTINGS

In order to reach service menu, first chose Channel, then press **"MENU"** buton, press **"Advanced Options"** then write "**4725"** by using remote controller.

You can see the service menu main screen below. You can check SW releases by using this menu under Diagnostic title. In addition, you can make changes on video settings, audio settings, DAP Parameters etc. using regarding titles. You may also use USB Operations for SW update and update Unique Keys and Configuration files.

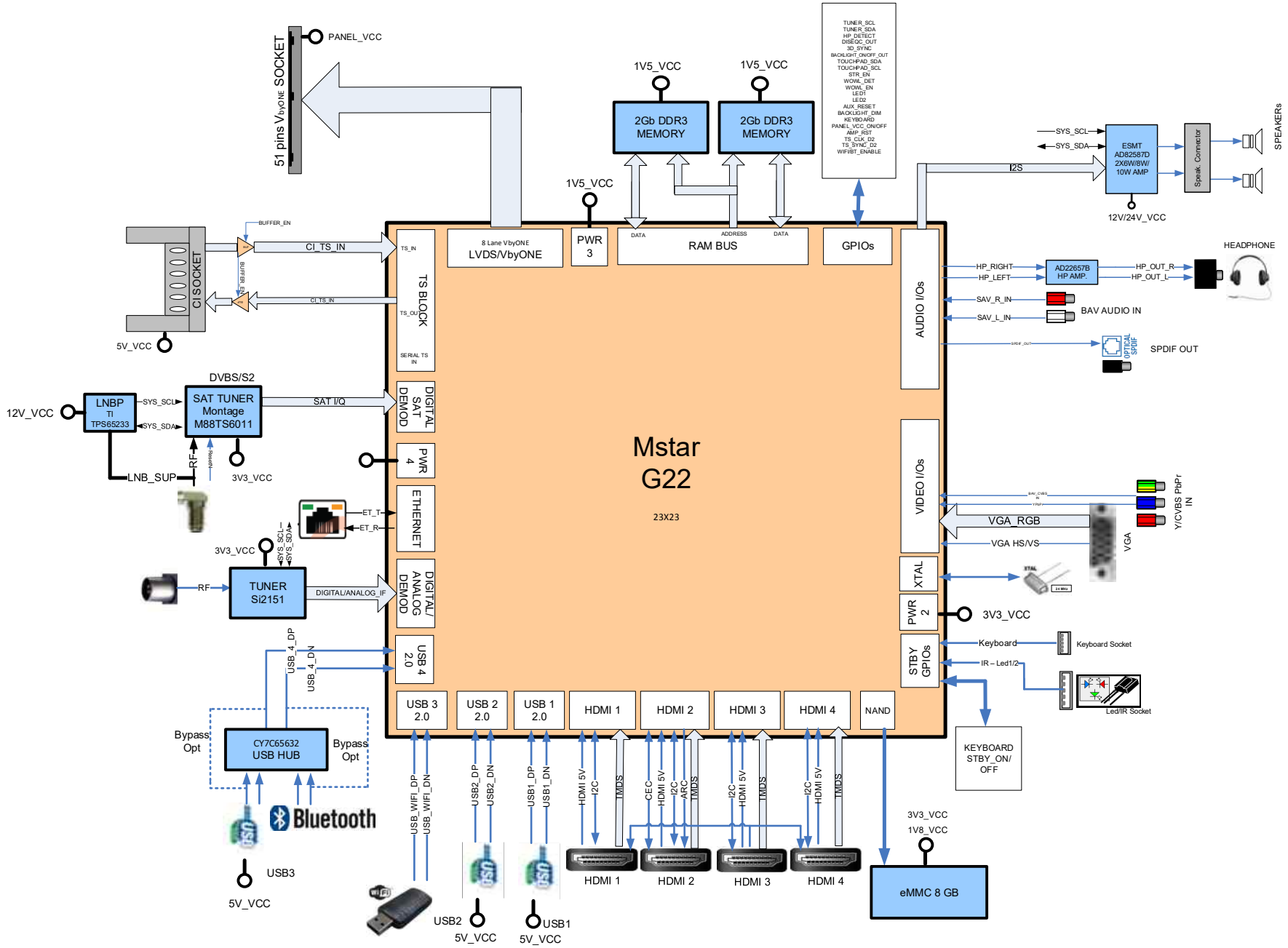


Service Menu



Diagnostic

14.GENERAL BLOCK DIAGRAM



15. PLACEMENT OF BLOCKS