//test bench

module tb\_moore1101\_74;

//inputs

reg rst;

reg din;

reg clk;

//outputs

wire y;

wire [2:0]pst;

wire [2:0]nst;

wire [3:0]count;

//instantiate the Unit Under Test (UUT)

moore1101\_74 uut(

.y(y),

.pst(pst),

.nst(nst),

.count(count),

.rst(rst),

.din(din),

.clk(clk)

);

initial begin

//initialize inputs

rst=1;

din=1;

clk=1;

#10 rst=0;

#10 din=0;

#10 din=1;

#10 din=1;

#10 din=0;

#10 din=1;

#10 din=1;

#10 din=1;

#10 din=0;

#10 din=1;

#50 $stop;

end

always

#5 clk=~clk;

endmodule