WITH PERFORMANCE REQUIREMENTS ON THE RISE, THE BENEFITS OF A CASCADED TOPOLOGY MAY OUTWEIGH ITS COMPLEXITY.

Cascaded power converters find acceptance as performance demands increase

Most of the popular power-conversion topologies—buck, boost, flyback, and forward—owe their status to a positive combination of performance and complexity. But as performance requirements for power conversion have increased over the years, topologies that were often overlooked because of their added complexity are now finding wide use. One example is the current-fed push-pull topology.

Avionics and military power converters have used the current-fed topology for a couple of decades. Current-fed push-pull is a "cascaded" topology, of which many varieties exist. This article examines several cascaded topologies that are part of the buck-regulator family.

To understand the current-fed push-pull topology, you first need to understand the voltage-fed push-pull converter (**Figure 1**). This converter comprises a buck regulator cascaded by a push-pull transformer-isolation stage. On the left side of the **figure** are the buck switch, freewheeling diode, and inductor. On the right side are the output capacitor and push-pull isolation transformer. If the push-pull isolation transformer had a turns ratio of 1-to-1, from a first-order point of view, all of the performance waveforms would be what you would expect for a buck regulator.

The actual operation is a bit more complex, but the device is still very much a buck regulator. Pulse-width modulation of the buck stage accomplishes the actual output voltage regulation. The push-and-pull switching devices run continuously, each switch alternating at a 50% duty cycle. Given ideal switches, you can view the push-pull stage as an ideal isolating dc-to-dc transfer stage with a gain equal to the transformer turns ratio. The transfer function for the buck stage, during continuous conduction, is $V_{PP}=V_{IN}*D$, where V_{PP} is the nominal voltage at the circuit midpoint (V_{PP}), and D is the buck-switch duty cycle. The transfer function for the push-pull stage is $V_{OUT}=V_{PP}/N$, where N is the transformer turns ratio. The composite transfer function of the two cascaded stages is then $V_{OUT}=V_{IN}*D/N$.

An example with ideal switches, a 2.5V output and an 8-to-1 (primary-to-secondary) transformer-turns ratio, would yield a voltage at $V_{PP}=20V$. A telecommunications input-voltage range of 36 to 72V would require an ideal buck-stage duty cycle

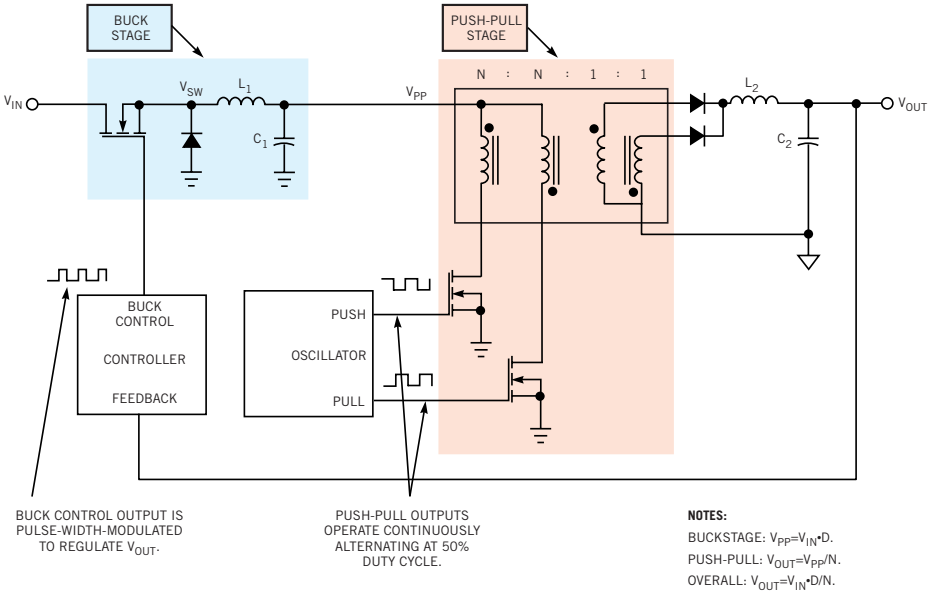


Figure 1 A voltage-fed push-pull converter comprises a buck regulator cascaded by a push-pull transformer-isolation stage.

from 55% (low line) to 28% (high line). The actual duty cycles would be a bit higher due to the switch-voltage drops, transformer resistance, and connection resistance. This duty-cycle range is comfortable for the buck stage. Sufficient dynamic range remains before the upper and lower duty-cycle limits, necessary for good transient response.

A close examination of the cascaded voltage-fed approach reveals that during the conversion process, the power is chopped and filtered twice. Two complete LC filters, the buck-stage output filter and the push-pull stage filter, accomplish the filtering. A simplification can add several performance benefits. Only one complete LC filter is necessary, leading to the current-fed push-pull approach (**Figure 2**). In the **figure**, the buck-stage output capacitor (C_1) and the push-pull stage inductor (L_2) have been removed to convert a voltage-fed converter into a current-fed push-pull converter. The approach is current-fed, because the push-pull stage now "feeds" directly from the buck inductor (current source). The transfer function and device-voltage stresses are the same for the voltage- and current-fed converter.

The push-and-pull switching devices each operate continuously, alternating at 180° out of phase. For proper operation of a voltage-fed push-pull stage, the actual duty cycle needs to be slightly less than 50%, so that both switches are never simultaneously on during transitions. If both switches are simultaneously on, excessive current will flow from the buck-stage output capacitor.

For proper operation of a current-fed push-pull stage, the push-pull duty cycles need to be slightly greater than 50%, creating a small overlap time in which both switching devices are on. Power to the push-pull stage is in the form of a current-fed current source formed by L_1. The push-pull overlap time is necessary to guarantee that there will always be a current path for the inductor current, even during the transition times between the push-pull switching events. Having no overlap time would require exact simultaneous switching between the push and the pull outputs, which is impractical. Further, a disruption in the current-source path during the switching event would result in a large voltage increase to the switching-device avalanche voltage.

Figure 3 shows the push-pull drain waveforms and the buck-stage switching node, V_{SW}. The overlap time is indicated when both drains are low. The **figure** also shows the operation of the buck stage, which operates at twice the frequency of either the push or the pull switching devices. Operating the transformer with both primary windings active during the brief overlap time does not present a problem for either the current source or the transformer. When both windings are active, the MMF (magnetomotive force) of the transformer breaks down, and the impedance on the V_{PP} node decreases toward zero. At that time, the inductor source current divides approximately equally between the primary windings.

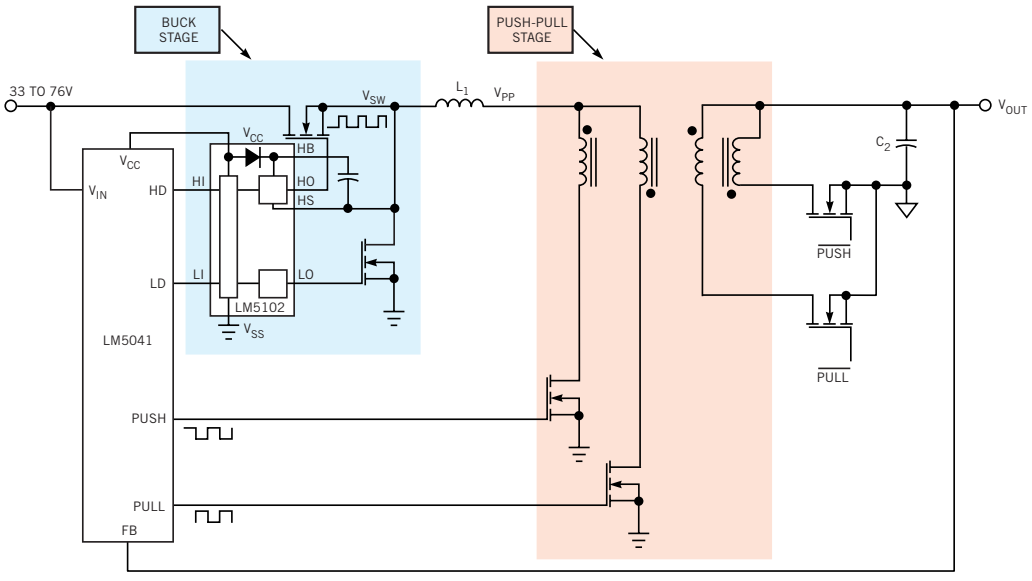


Figure 2 In this current-fed, cascaded buck and push-pull power converter, which offers a favorable topology for multiple-output converters, the push and pull outputs operate continuously, alternating with a slight overlap. The buck stage, which operates at twice the push-pull frequency, controls the output voltage. Continuous output current from the push-pull stage requires minimal filtering, and low push-pull switching losses and matched synchronous-rectifier loading achieve high efficiency.

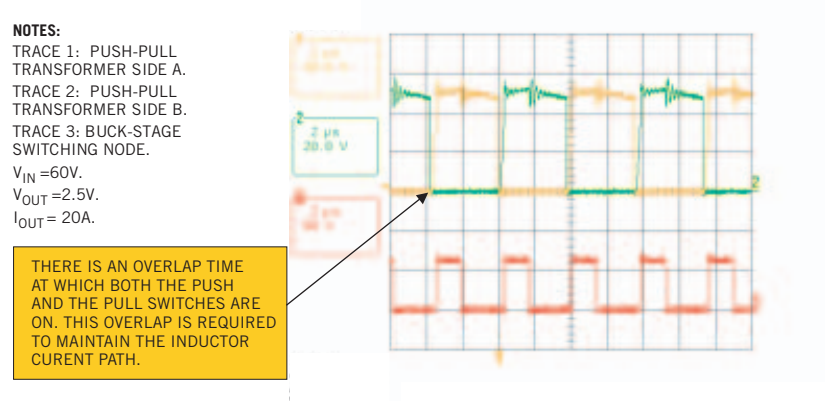


Figure 3 Switching waveforms for cascaded buck and push-pull power converters indicate an overlap time when both drains are low.

Some switching-loss reduction occurs in the push-pull stage when a power converter is configured as a current-fed converter, because device-switching loss requires the presence of both voltage and current.

Figure 4 shows the drain voltage and current for the push-pull devices. Current transitions occur in 50% increments from 100 to 50 to 0%; at the overlap time, when both devices are on, each device carries half the current. An interesting benefit of this situation is that for a given turn-on or -off event, voltage is present across the switching device for only 50% of the current transition. The portion of the switching event with zero voltage across the device results in greatly reduced switching losses. Also important, the off-state voltage stress on the push-pull devices is V_{OUT}*N*2 (ignoring leakage-inductance spikes) for all input voltages. The buck stage essentially acts as a preregulator for the push-pull stage. This preregulation allows the use of lower voltage devices than when you use a conventional push-pull power converter, whose primary switching devices see off-state voltage stresses of V_{IN}*2.

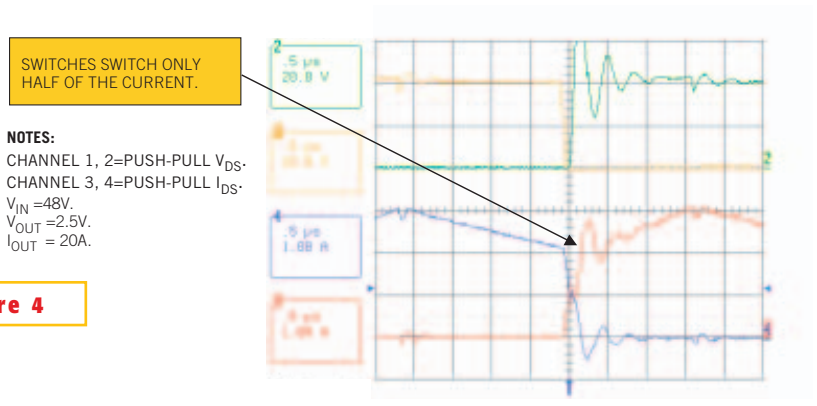


Figure 4

Drain voltages and currents for the push-pull devices indicate that current transitions occur in 50% increments, from 100 to 50 to 0%; because of the overlap time when both devices are on, each device carries half the current.

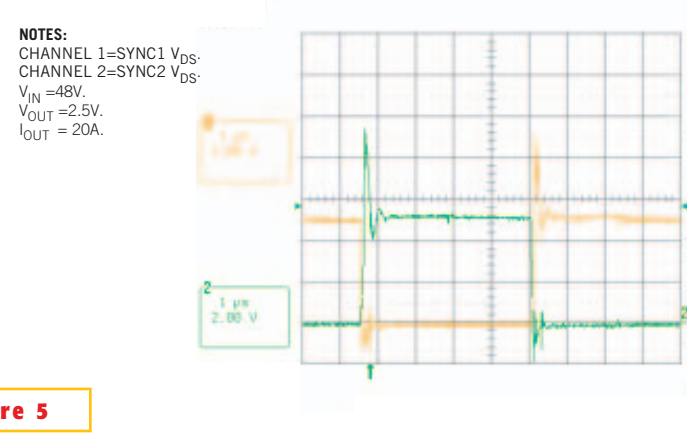


Figure 5

Synchronous rectifiers need to operate with dead time between the switching transitions. If they were both on at the same time, excessive current would flow form the output capacitor.

The current-fed push-pull approach yields the greatest benefit in low-voltage, high-current applications. In these applications, losses in the secondary rectification dominate the power-loss budget, and optimized synchronous rectification is mandatory to achieve high efficiency. The first topology benefit for the synchronous rectifiers is that, unlike other topologies, the off-state voltage stress on the synchronous rectifiers is minimized to V_{OUT}*2 throughout the entire input-voltage range. For the same reason, the buck stage acts as a preregulator, reducing the input voltage to the push-pull stage, V_{PP}. This reduced voltage stress allows the use of low-voltage, ultralow-on-resistance devices to implement the synchronous rectifiers. Another topology benefit of using synchronous rectifiers is that each device continuously operates at almost 50% duty cycle for all line and load conditions, ensuring that the devices will share an equal thermal load. Both of these benefits either allow the use of smaller, less expensive devices or greatly increase performance.

Table 1 compares the synchronous-rectifier stresses for a representative 3.3V-output power converter using forward, conventional push-pull, and current-fed push-pull topologies. The current-fed push-pull synchronous rectifiers have the lowest operational voltage stress. Each of the two rectifiers devices operate for 50% duty cycle for all line-input voltages, guaranteeing equal thermal loading and no requirement to overdesign the devices for varying operational duty cycles.

Figure 5 shows the synchronous-rectifier V_{DS} waveforms for a 2.5V-output current-fed push-pull. Note that the synchronous rectifiers must operate with dead time between the switching transitions. If they were both on at the same time, excessive current would flow from the output capacitor. You can configure

TABLE 1–TOPOLOGY COMPARISON OF SYNCHRONOUS-RECTIFIER STRESSES

Topology	Rectifier-voltage stresses	Example: 3.3V out, 35 to 80V input (V)	Example: assumptions
Forward	V_{IN}*(N_S/N_P)	20	High line with 4-to-1 transformer ratio
Push-pull	V_{IN}*(N_S/N_P)*2	26.7	High line with 6-to-1 transformer ratio
Cascaded push-pull	V_{OUT}*2	6.6	All line conditions with 6-to-1 transformer ratio
Topology	**Rectifier current ratios**	**Example: 3.3V out, 35 to 80V input (%)**	**Example: assumptions**
Forward	I_{OUT}*D and I_{OUT}*(1-D)	16/84	Ratio at high line
Push-pull	50%*I_{OUT}	50	All line conditions
Cascaded push-pull	50%*I_{OUT}	50	All line conditions

the sync rectifiers in a control-driven manner using the inverted control signals from the push-pull stage shown in **Figure 2**.

The current-fed push-pull topology provides tighter voltage cross regulation for multiple output applications. Unlike the forward and conventional push-pull topologies, which are also in the buck family, the current-fed approach offers outstanding cross-regulation and transient properties at reduced cost and complexity. The individual inductor for each output in the forward topology causes mismatching on cross-regulation and tends to isolate the

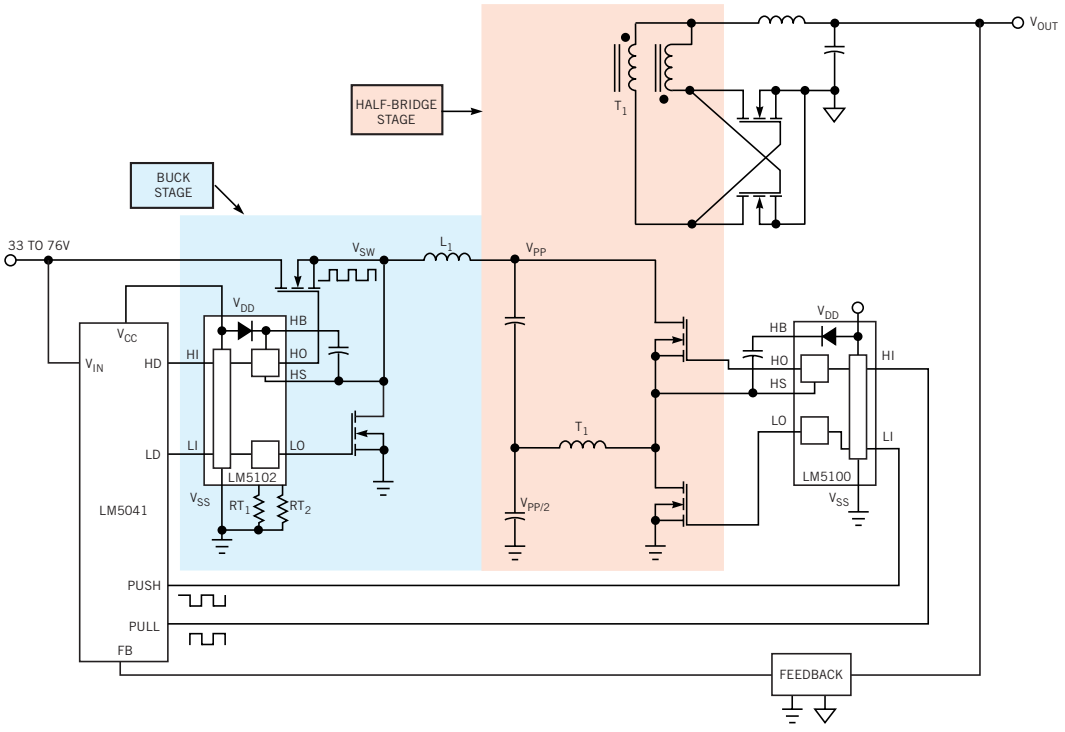
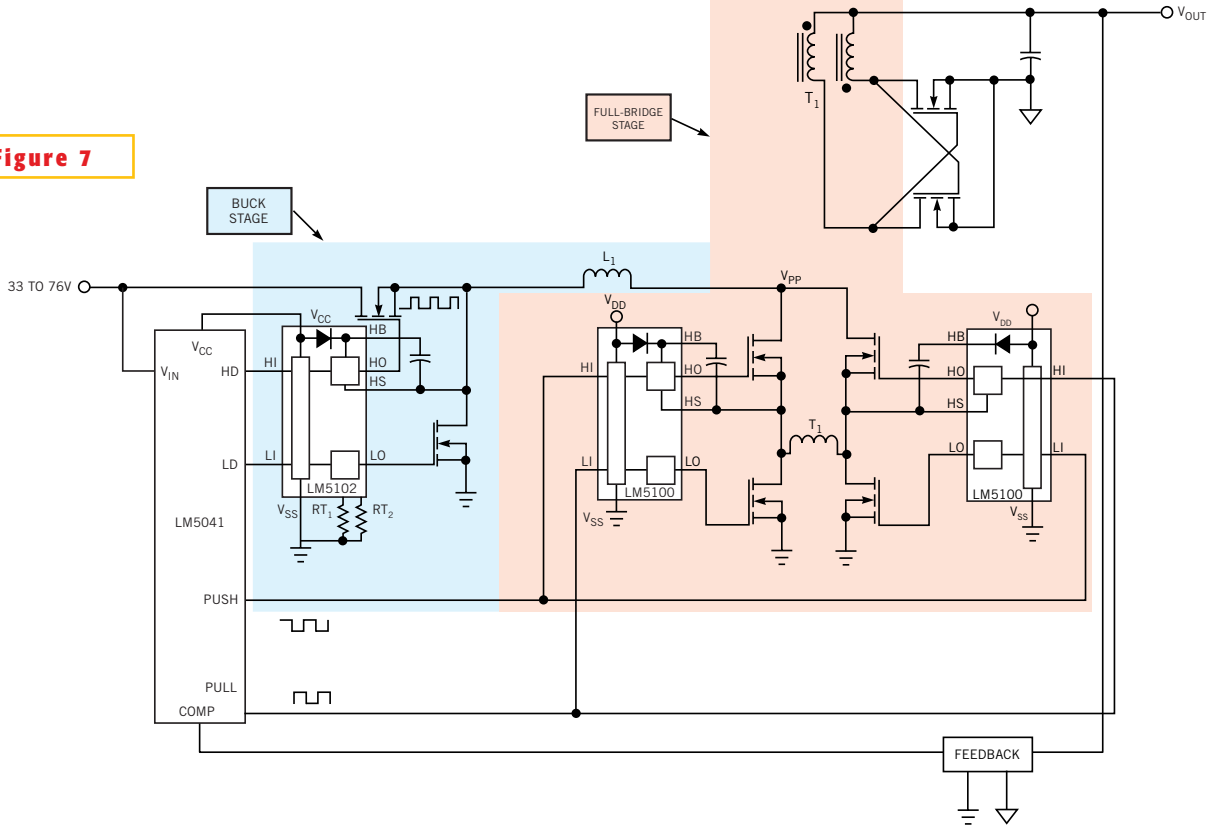


Figure 6 The buck-stage output of this cascaded half-bridge power converter is configured with an output inductor and a set of capacitors, which act both as an output capacitor for the buck stage and as voltage divide-by-2 for the half-bridge stage.

Figure 7



The buck-stage output inductor in this cascaded, full-bridge power converter defines the approach as current-fed.

outputs from one another. Although coupled inductors can help, many second-order difficulties remain. With the current-fed approach, all of the outputs share a single inductor on the primary side. Further, with the inductor located on the primary side, there is a reduction in high current connection and I^2*R losses. This single-inductor approach results in cross-regulation and transient performance more like a flyback topology. The current-fed topology offers excellent cross-regulation during transient events; the output capacitors of all the outputs are essentially in parallel and act to supply additional transient energy when necessary.

The continuous operation of the push-pull isolation stage optimizes the transformer-core usage and provides equal power dissipation among the primary and secondary switches. A push-pull transformer operates in two quadrants of the flux density/magnetizing force (BH) curve and can be half the size for a given power of a transformer operated in a single quadrant.

You can extend the cascaded approach to half- and full-bridge power converters. Both the half- and full-bridge approaches contain the buck-stage preregulator cascaded with an isolation/step-down transformer. **Figure 6** shows a cascaded half-bridge power converter. The buck-stage output is configured with an output inductor and a set of capacitors, which act both as an output capacitor for the buck stage and a voltage divide-by-2 for the half-bridge stage. The inclusion of these capacitors defines the approach as voltage-fed. The advantages of the half-bridge over the push-pull approach are a factor-of-2 peak-voltage reduction of the primary switching devices and more room in the transformer-winding window area, because there is only a single primary winding. The drawbacks are the added complexity of the transformer high-side gate driver and the addition of the voltage-splitter capacitors and a small output inductor.

Figure 7 shows a cascaded, full-bridge power converter. The buck-stage output inductor defines this approach as current-fed. The four primary transistors are driven diagonally at just over 50% duty cycle. In this manner, overlap is realized at the transitions necessary for a current-fed approach. The current-fed full-bridge finds use in the higher power levels. The advantages are similar to those of the half-bridge except that the current per primary switch is half that of half-bridge approach. The drawback is the added complexity of the two high-side gate drivers. However, modern integrated gate-driver/level-shifter devices have driven down the cost and complexity issues for high-side gate drive.□

Author's biography

Robert Bell is principal applications engineer at National Semiconductor Corp (Phoenix). In his current position, he defines next-generation power converters, PWM controllers, gate drivers, and support ICs and associated application circuits. He received a BSEE from Fairleigh Dickinson University (Teaneck, NJ). His interests include hiking, camping, and playing tennis.