CRYSTAL OSCILLATOR CIRCUITS

An oscillator circuit requires that two conditions be satisfied: that it contains an amplifier having sufficient gain to overcome the loss due to its feedback network, and that the phase shift around the whole loop is zero at the wanted frequency. It must be ensured also that the loop gain at other frequencies where the phase shift might be zero, is less than that at the wanted frequency. For example a crystal oscillator which is intended to operate at the crystal's third overtone frequency could do so otherwise at its fundamental.

When power is first applied to an oscillator the signal amplitude builds up until it is limited by the non-linearity of its maintaining amplifier or, by an external level-control circuit. In the former case, the limiting method employed by all but high-precision oscillators, the output waveform is therefore dependent upon the type of amplifier and its method of limiting, and the point of signal extraction. Any point in the circuit can be chosen to extract the signal as long as impedance levels are borne in mind. It is important that any loading be as light as possible in order to maintain a high circuit Q and, thereby, good short-term stability and low phase noise.

The Circuit Condition

Some of the circuits to be illustrated require crystal calibration at series resonance, while others require load-resonance calibration with a stated load capacitance value. The appropriate circuit condition must be stated when ordering crystals or, while they will oscillate, they will not do so at precisely the desired and marked frequency.

Below 150.0kHz

The relatively high equivalent series resistance of crystals in this frequency range demands a high amplifier gain. This can be provided as shown in Fig.9 by employing two cascaded common emitter bipolar stages. Component values are indicated for frequencies down to 50kHz.

The diodes D1 and D2 in the collector circuit of TR1 limit the crystal drive level to avoid damage and the tuned circuit in the collector of TR2 adds some selectivity. The crystal should be calibrated at load resonance with the mid value of the trimmer capacitor C2. Series-resonance calibration is recommended only if precise frequency trimming is not required as only a limited pulling range is afforded by adjustment of L1.

150.0 to 550.0kHz

DT and CT are the usual cuts for conventional crystals in this frequency range, for which a suitable circuit for those calibrated at series resonance is shown in Fig. 10. These cuts have a strong mode at about twice the wanted frequency which should not cause a problem.

L1, which must be initially adjusted for oscillation near the crystal frequency with the crystal shorted, may be used as a fine frequency trimmer. Series resonance crystal calibration should be specified but parallel resonant crystals may be used if C1 is replaced by a capacitor whose value is

Fig. 9

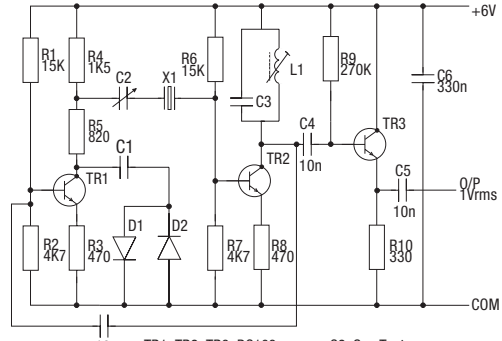
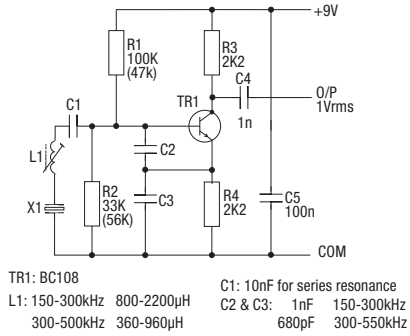


Fig. 10



APPLICATION NOTES

equal to the crystal load capacitance.

0.95 to 21.0MHz

The circuit shown in Fig.11 is designed for use with high stability AT-cut fundamental mode crystals calibrated at load resonance. Specify 30pF load capacitance 950kHz to 10MHz and 20pF for 10 to 21MHz.

15.0 to 105.0MHz

Figs.12 and 13 give circuits suitable for operation with 15 to 63MHz third and 50 to 105MHz fifth overtone series resonant crystals respectively. A small positive frequency offset, +20ppm, will allow a wide trimming range.

When ordering an overtone crystal, reference must not be made to its fundamental frequency since it is not an exact sub-multiple of the overtone frequency. Overtone crystals are produced and calibrated specifically for operation at their marked frequencies.

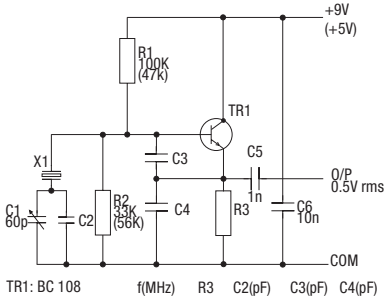
By including a tuned circuit at twice or three times the crystal frequency in the collector TR1 of these circuits, it is possible to extract, from the collector, harmonics of the crystal frequency. Such an approach offers an easy and economical solution to VHF crystal oscillator design.

Above 105.0MHz

The low reactance of stray circuit capacitances at these high frequencies can make a reliable oscillator design difficult to achieve. To help prevent oscillation not controlled by the crystal, the static capacitance Co of the crystal is often tuned out with a small parallel inductance – L2 in Fig.14. L1 in the circuit is tuned for maximum output but it can also serve a fine frequency trimmer. Alternatively, the frequency can be trimmed by inserting variable reactance in series with the crystal.

At these frequencies, it may be necessary to obtain correlation of the oscillator frequency with crystal frequency as measured by the crystal manufacturer. If high accuracy is required therefore, it is important to experiment with a sample crystal on which the manufacturer's precise frequency reading is known. Any discrepancy between the crystal and oscillator frequencies can then be remedied by

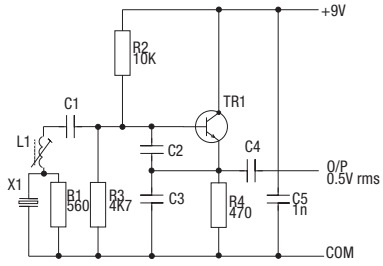
Fig. 11



TR1: BC 108

f(MHz)	R3	C2(pF)	C3(pF)	C4(pF)
0.95-3	3K3	not used	220	220
3-6	3K3	33	150	150
6-10	2K2	33	150	150
10-18	1K2	not used	100	100
18-21	680	not used	68	33

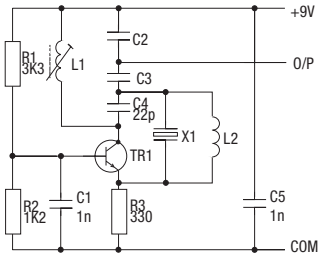
Fig. 12



TR1: BC 108
L1: 0.5µH - 3.0µH

f(MHz)	C1(pF)	C2(pF)	C3(pF)	C4(pF)
15-10	100	100	68	33
20-26	100	100	68	33
26-48	100	68	47	33
48-63	68	33	15	15

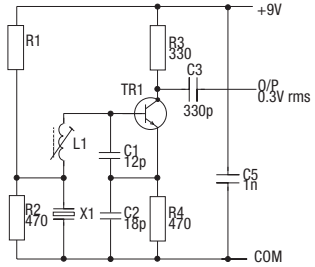
Fig. 14



TR1: BF 180

$\frac{C2.C3}{C2+C3} = 10pF$ Adjust the ratio to suit following circuit $L1 = \frac{1}{\omega^2.7pF}$ $L2 = \frac{1}{\omega.C_o}$

Fig. 13



TR1: BF 180
L1: 0.3µH-1.5µH

R1: 2K7 50-80MHz
1K2 80-105MHz

calling for an offset calibration tolerance for further crystal supplies.

TTL Clock Oscillators

Many circuits have appeared over the years that use TTL inverters and gates as the active elements. Often, such designs are prone to oscillate at unwanted frequencies or, for a variety of reasons, do not operate properly. Even certain integrated circuits which have been designed specifically for the purpose can be troublesome. As a general rule, extensive testing should be done on these circuits to make sure that the design is not marginal and will not result in belated problems.

Figs.16 to 18 illustrate some possible arrangements for use with the 7400, 7402, 7404 etc. Unused inputs of NAND gates should be connected to the positive supply and those of NOR types, to earth. The approximate frequency ranges shown apply only to standard TTL ICs; although with higher value bias resistors in Figs.16 and 17, the low power families can be used to advantage. In these two circuits, the value of C1 and C2 if found to be necessary, should be determined experimentally. For the frequency range 4 to 14MHz, the circuit of Fig.18 will give good results.

TTL gate circuits cannot be fully recommended if the highest stability is required. Random phase shift within the IC will cause jitter and the relatively high crystal drive level does not make for good long-term stability.

A conventional discrete component oscillator such as one already described, followed by a buffer amplifier provides a better way of obtaining a stable design. A suitable buffer is shown in Fig.15 in which the resistor R2 decouples the supply to the oscillator. The insert shows a Complimentary version of the buffer amplifier which can be used for a faster rise time when feeding capacitive loads. For operation of the circuits of Figs. 10 and 11 from a 5V supply, the values for R1 and R2 shown in brackets should be used. In order to reduce the output to a level suitable for the logic buffer, reduce R3 in Fig.9; and increase C3 and C4 in Fig.11. For the latter circuit, crystals calibrated for 30pF load capacitance can now be specified for use up to about 15MHz.

Fig. 15

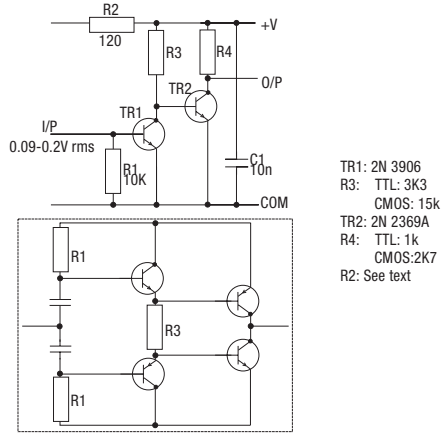


Fig. 16

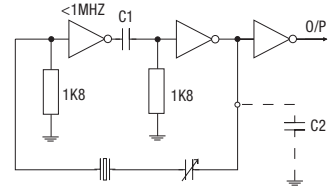


Fig. 17

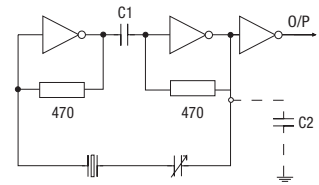
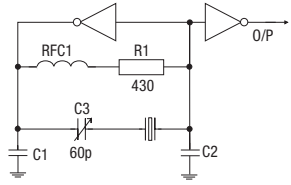


Fig. 18



f1(MHz)	C1 (pF)	C2 (pF)	RFC1 (µH)
4.0 - 6.0	330	220	100
6.0 - 9.0	330	180	68
9.0 - 11.5	220	150	39
11.5 - 14.0	330	120	22

CMOS Clock Oscillators

Fig.19 shows the circuit of a typical CMOS inverter oscillator in which the crystal is connected in a pi-network and operates at load resonance. Again, only one gate input is connected to the crystal; unused inputs are tied to the appropriate supply rail. Simple formulae for calculating the values of Ca, Cb and R are given which will result in a reliable 4000UB-series design for use up to about 3MHz. However, the actual values used may differ slightly owing to variations in the stray capacitances of individual layouts. If frequency trimming is required, a trimmer capacitor can be fitted in parallel with Cb and the fixed capacitor reduced accordingly.

If connections to the sources of each FET in the inverter are available, as in a 4007, the resistor value calculated for R may be inserted at these points, the single series resistor being no longer used. This arrangement, which is illustrated in Fig.20 gives better stability than the standard configuration due to negative feedback.

For operation above 3MHz, the resistor R is omitted and the crystal connected directly between the inverter input and output. The two pi-network capacitors will now have the same value and their series combination plus inverter capacitances and strays will be equal to CL. Low values of CL, for example 12pF, and/or a high supply voltage may be necessary for reliable operation.

If preferred, a discrete component oscillator together with the logic buffer of Fig.16 can be used. The power consumption however will be considerably greater than that of a CMOS inverter oscillator.

Frequencies 20.0 to 200.0MHz

The schematic of this VHF overtone oscillator is shown in Figs.21 & 22. The crystal operates at its overtone and is tapped into the capacitive side of the LC tank circuit. The circuit has no parasitic effects of any kind.

There are no 2.6V zener diodes available, so four signal diodes are cascaded in series for base biasing. The emitter's output resistance that drives the crystal is 25ohms. The crystal load impedance is mostly capacitive and is one or two times the impedance of C_2 (35ohms), depending on

Fig. 19

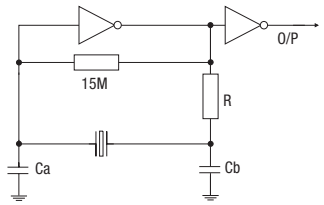


Fig. 20

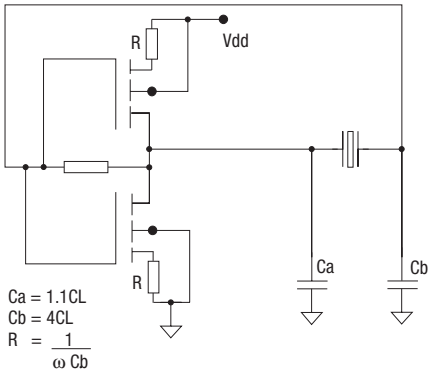


Fig. 21

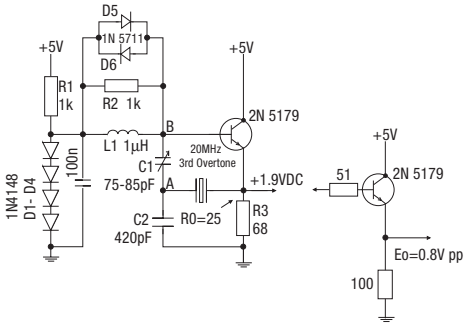
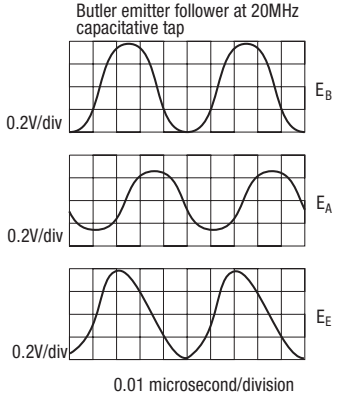


Fig. 22



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the value of C. The crystals internal series resistance R_1 is between 30 and 40ohms.

The circuit works very well and the absence of parasitics is a big help. By tuning C, the oscillation frequency can be set either at or slightly above (2ppm) the series resonance.

Figs.23 & 24 show typical values for 50MHz and 100MHz operation.

Integrated Circuits as Oscillators

A large number of integrated circuits are available for use as an oscillator or include a crystal oscillator. Many existing IC's require only the attachment of an external crystal while some require other components as well. There are three main types of oscillator, the first provides a single bipolar or field effect transistor to which the external crystal and feedback network can be attached. For this class of circuit the designs shown for transistor oscillators are directly applicable and the frequency stability is generally good.

The second class of circuit, often using MOS technology, provides a gate which can be used as a crystal oscillator. The frequency stability is generally equivalent to that of oscillators using discrete gates of the same type.

The third class of circuit is designed with a multi-stage amplifier on the chip and the external crystal either closes the feedback path from the amplifier output to its input or it serves as a frequency-selective by-pass at some point in the amplifier. Many of these circuits are used as clock drivers for microprocessors, as frequency synthesizers, modems, TV circuits, phase-locked loops and the like. As might be expected, the frequency stability varies greatly with the design and while some are good, others are very poor indeed.

While it is desirable in the design of integrated circuit oscillators to use a set of analytical tools, the detailed equations for oscillation are generally too complex to be useful. Two approaches are presented here based on the terminal parameters of the integrated circuit. In those circuits where the crystal acts as a frequency-selective by-pass in the amplifier which is internally cross-coupled, it may be convenient to think of the circuit as a negative-resistive element in series with an inductance and a series compensating capacitor C in series with the crystal. For on-frequency operation with a series resonant crystal, C should be resonant with Lo at the nominal frequency of the crystal. The resistance Rn is a negative value and must be larger in magnitude than the equivalent resistance of the crystal for oscillation to take place.

It is possible to determine the magnitude of Rn in several ways. Perhaps the most obvious is to place a crystal between the appropriate terminals of the IC and add series resistance until oscillation will no longer occur. The magnitude of the negative resistance is then given by the sum of the crystal resistance and the additional series resistance. The magnitude of the oscillator inductance can be found by noting the difference between the frequency of oscillation and the series resonant frequency of the crystal (without C or the series resistance) and calculating.

Fig. 23

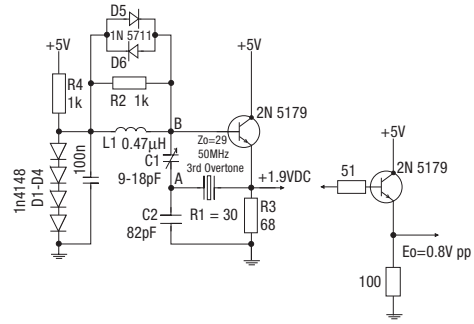
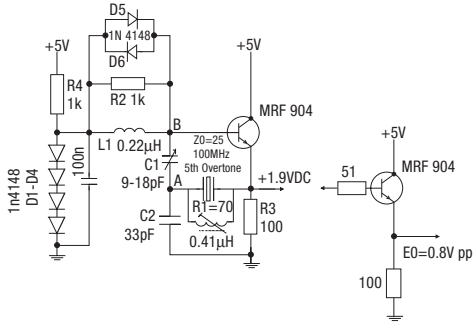


Fig. 24



It can also be found experimentally by selecting C to obtain the series resonant frequency of the crystal. Then:

$$L_O = \frac{1}{(2\pi_{fs})^2 C}$$

Since the equivalent inductance will in general vary as a function of frequency it should be computed near the nominal frequency of the crystal used.

It is desirable to minimize the equivalent inductance of an oscillator for several reasons. First the equivalent inductance of an oscillator will change with temperature and supply voltage, causing the oscillator frequency to drift. Secondly, it may result in free-running oscillations through Co of the crystal.

The equivalent inductance is a result of phase shift in the amplifier and can be minimized in the design by using as few stages as possible and by increasing bandwidth of the amplifier. The negative resistance will of course be a function of the gain of the amplifier and the impedance level where the crystal is placed.

Test data on several IC's of the cross-coupled type shows a wide variation in the equivalent inductance, from approximately 1- 2µH to greater than 250µH over the frequency range from 1 to 20MHz. Therefore, while some IC's operate with the crystal near series resonance, others operate as much as 1% low in frequency.

Frequencies 1 to 20MHz

The schematic circuit for this series resonant oscillator at 1MHz is shown in Fig. 25. The circuit waveforms are shown in Fig.26. This circuit has outstanding performance and works very nicely off a 5V supply. Waveforms at the crystal are very good. The frequency changes very little when power supply voltage or temperature are changed. The low ECL drive voltage keeps crystal dissipation low and the low ECL drive resistance R_L, which gives very good frequency stability. The ECL receiver format is well adapted to high frequency oscillator circuits. At high frequencies crystals are low impedance devices and ECL circuits can drive low impedance loads down to 50Ω easily. Input resistances of ECL circuits are high and they are also linear over the ECL voltage range. As shown in Fig.26 the crystals square wave drive waveform at Pin 3 has a definite slope during transition between binary states, indicating the ECL unit is operating as a linear amplifier during the transition interval.

Fig.27 shows the circuit at 20MHz. The crystals internal series resistance R_1 is 7Ω; the crystals load resistance R_L is 10Ω. At 20MHz the ECL receiver has to be able to drive a 17Ω load (R_1+R_L=12Ω), a very low value. The receivers output resistance is controlled by the ECL emitters output current, which is in turn controlled by the emitters pull-down resistor R_3. R_3=510Ω works well at 1MHz but has to be decreased to 100Ω at 20MHz to get the ECL output resistance down low enough to provide a reasonable drive waveform to the crystal.

There are three ECL receivers in one DIP. One of the two unused ones could be used as a no-cost buffer between the

Fig. 25

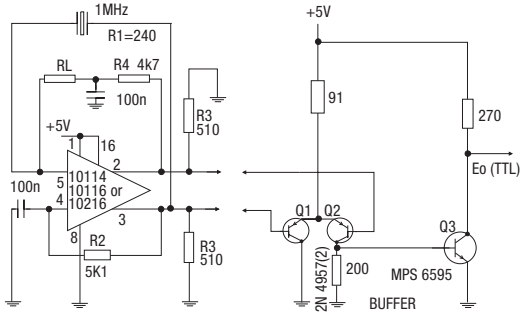


Fig. 26

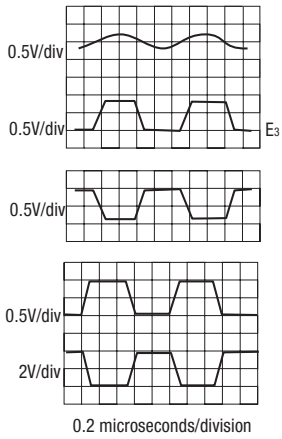
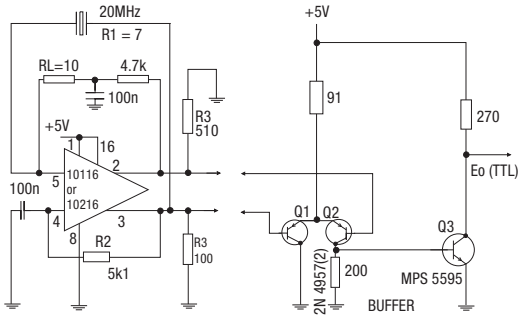


Fig. 27



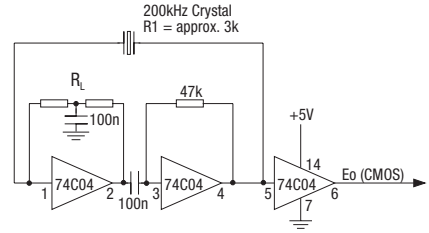
oscillator and the two transistor buffer, but the circuit will oscillate spuriously when the crystal is removed. Because of this the ECL receiver should not be used as a buffer.

Frequencies up to 500kHz (CMOS)

Each inverter in Fig.28 has negative feedback round it to ensure that it is biased in the middle of its linear region, so that oscillation will always start when power is applied. The feedback resistor round the first inverter is divided into two series resistors and the centre point is bypassed to ground. R_L is used as the crystals load resistor and is set equal to or somewhat less than the crystals internal series resistance R_1. Figs.29 & 30 shows good waveform at the crystal. The spikes on the crystal sine wave output appear to be due to sharp edges of the crystals square wave drive feeding through on the crystals shunt terminal capacitance CO.

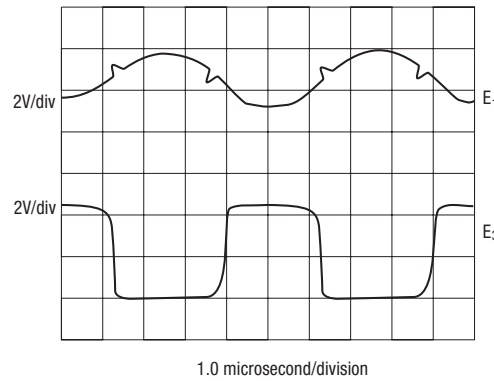
The overall performance of this oscillator is average with on/off times of 2.45µsec to 2.55µsecs. This is due to its frequency sensitivity to power supply voltage changes being higher than it should be. This high sensitivity to power supply voltage changes seems to be characteristic of most CMOS IC's.

Fig. 28



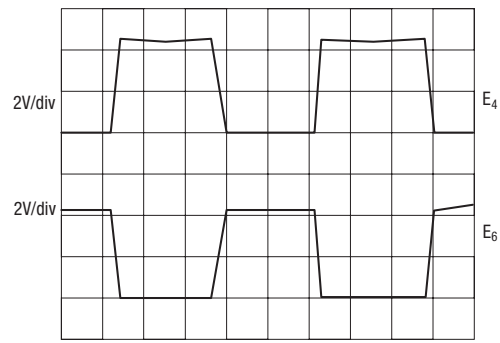
Note: Not suitable for miniature crystals

Fig. 29



1.0 microsecond/division

Fig. 30



1.0 microsecond/division