OZ890 DATASHEET

Version 1.6

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Battery Pack Protection and Monitor IC

FEATURES

- **Supports 5-13 Series Li-ion and Li-polymer Battery Cells or 20/30 Series NiMH battery Cells**
- **Multi-channel ADC for current, voltage and temperature measurement**
  - 13 channels for cell voltage measurement (signed 13 bits)
  - 2 channels for 20S NiMH cell voltage measurement (signed 13 bits), when configured to 20S NiMH
  - 3 channels for 30S NiMH cell voltage measurement (signed 13 bits), when configured to 30S NiMH
  - 1 channel for current measurement (signed 16 bits, accuracy down to 2.1nVhr)
  - 1 channel for internal temperature measurement (signed 13 bits)
  - 3 channels reserved for customer specific applications (one programmable 13-16bits; two 13bits)
- **Built-in 2-level protections**
  - First level protection
    - ✓ Over voltage (OV)
    - ✓ Under voltage (UV)
    - ✓ Over current (OC)
    - ✓ Short circuit (SC)
    - ✓ Over temperature (OT)
    - ✓ Under temperature (UT)
  - Second level Permanent Failure (PF) protection, each PF mode can be enabled individually by properly setting EEPROM
    - ✓ Extremely high voltage PF (VHPF)
    - ✓ Extremely low voltage PF (VLPF)
    - ✓ Cell voltage Unbalance PF (CUPF)
    - ✓ MOSFET Failure PF (MFPF)
    - ✓ Deadman PF (DMPF) (Software Mode only)
- **Embedded 64X16Bits EEPROM (**EEPROM write/erase life cycle is about 100000 times at ambient temperature 25°C) **for programmable protection thresholds and variable threshold detection / release delay time**
- **Supports Internal/External Bleeding for Cell balance**
- **Supports Hardware Mode (without Microprocessor) or Software Mode (with Microprocessor)**
- **Embedded voltage based capacity (gas) gauge (V-GG) function**
- **Supports separate charge and discharge protection loop**
- **Integrated 2.5V, 3.3V and 12V voltage regulators**
- **Integrated MOSFET driver**
- **Supports PWM discharge (for power tools application)**
- **Supports I^2C serial Interface**
- **Supports battery authentication for better security**
- **Low power consumption**

APPLICATIONS

- **Electric Bicycle / Electric Motorcycle**
- **Power Tools**
- **UPS backup battery**
- **Electric Vehicles (EV/HEV/PHEV)**

GENERAL DESCRIPTION

OZ890 is a highly integrated battery pack protection and monitor IC for managing Li-Ion or NiMH battery pack in electric bicycle, electric motorcycle, power tools, and UPS applications. It supports 5-13 (4-Bit EEPROM configuration) series Li-Ion battery pack or 20/30 series NiMH battery pack applications.

In Li-ion battery pack applications, the integrated protection circuits work constantly to monitor each cell's voltage, the charge/discharge current and the pack temperature to provide over-voltage, under-voltage, over-current, short circuit, over-temperature and under-temperature safety protection. Working with embedded MOSFET driver circuits, the protection circuits will independently shut off the MOSFETs if necessary. When cell voltage is higher than the pre-set maximum rating voltage or lower than pre-set lowest working voltage, or cell voltage unbalance is larger than the pre-set maximum value, or the leakage current is bigger than the pre-set values while the corresponding MOSFET is off, OZ890 can automatically assert the Permanent Failure (PF) signal to blow an external fuse. The PF signal also can be used to drive an LED to signal an alarm to user. All of the protection thresholds and their related delay time are programmable through the settings in EEPROM for different battery types and the needs of actual applications.

With integrated multi-channel 16-bit ADC, OZ890 measures the voltage, current and temperature of the battery pack sequentially, and implements a

simple voltage based battery capacity (gas) gauge (V-GG). With the option of working with O_2Micro's gas gauge Microprocessor or other general MCU, a more accurate coulomb counting capacity (gas) gauge function can be implemented.

OZ890 supports internal/external bleeding for cell voltage balance during the charging state or idle state (no charge and discharge current state), ensuring longer battery cycle life.

OZ890 can be configured (1 bit) to work in Hardware Mode (without Microprocessor) or Software Mode (with Microprocessor) using the embedded EEPROM (1 bit). In Hardware Mode OZ890 can work independently for Li-Ion or NiMH battery pack protection and monitoring. In Software Mode, OZ890 can work with an external Microprocessor to implement a more accurate coulomb counting gas gauge function or other dedicated functions. In Software Mode, some functions of the protection engine and state machine can be controlled by Microprocessor.

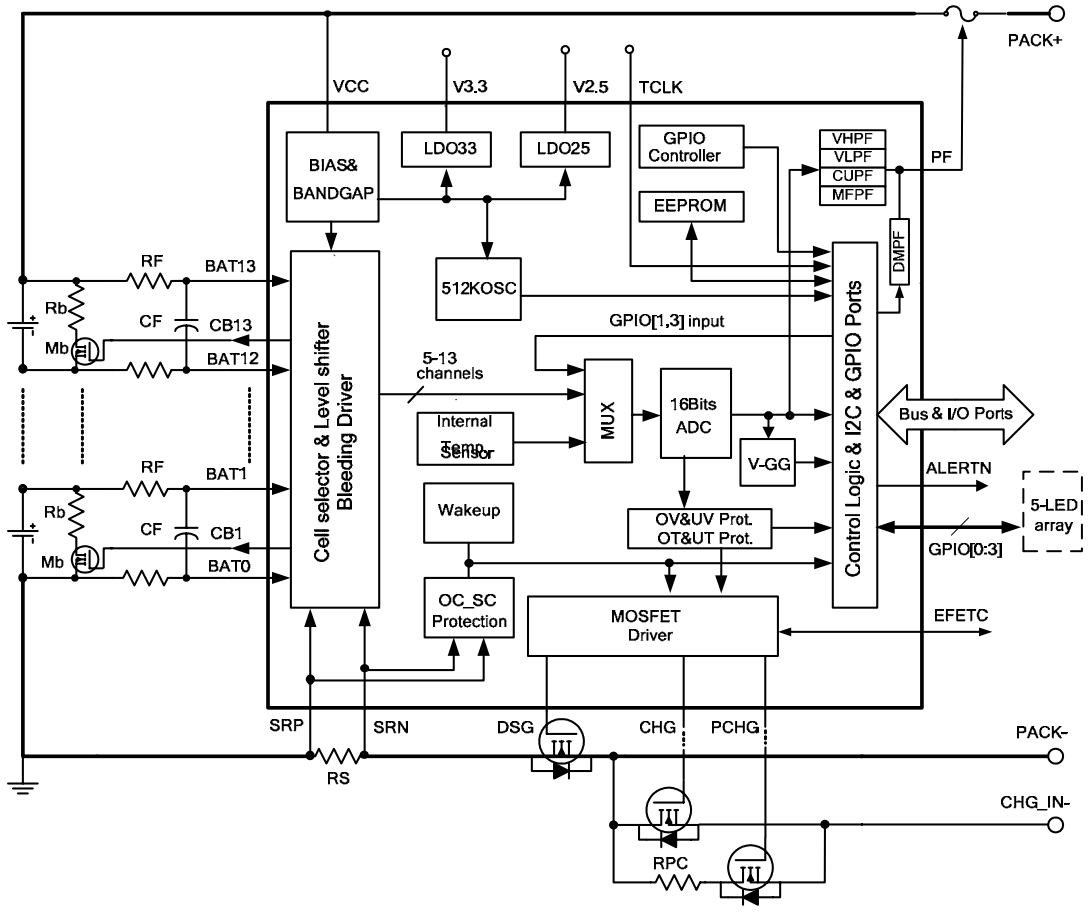
Note *For use of OZ890 with a microcontroller "software mode" please refer to application note "AN-6" and consult with O2Micro's Field Application Engineer for additional materials that may be available.*

ORDERING INFORMATION

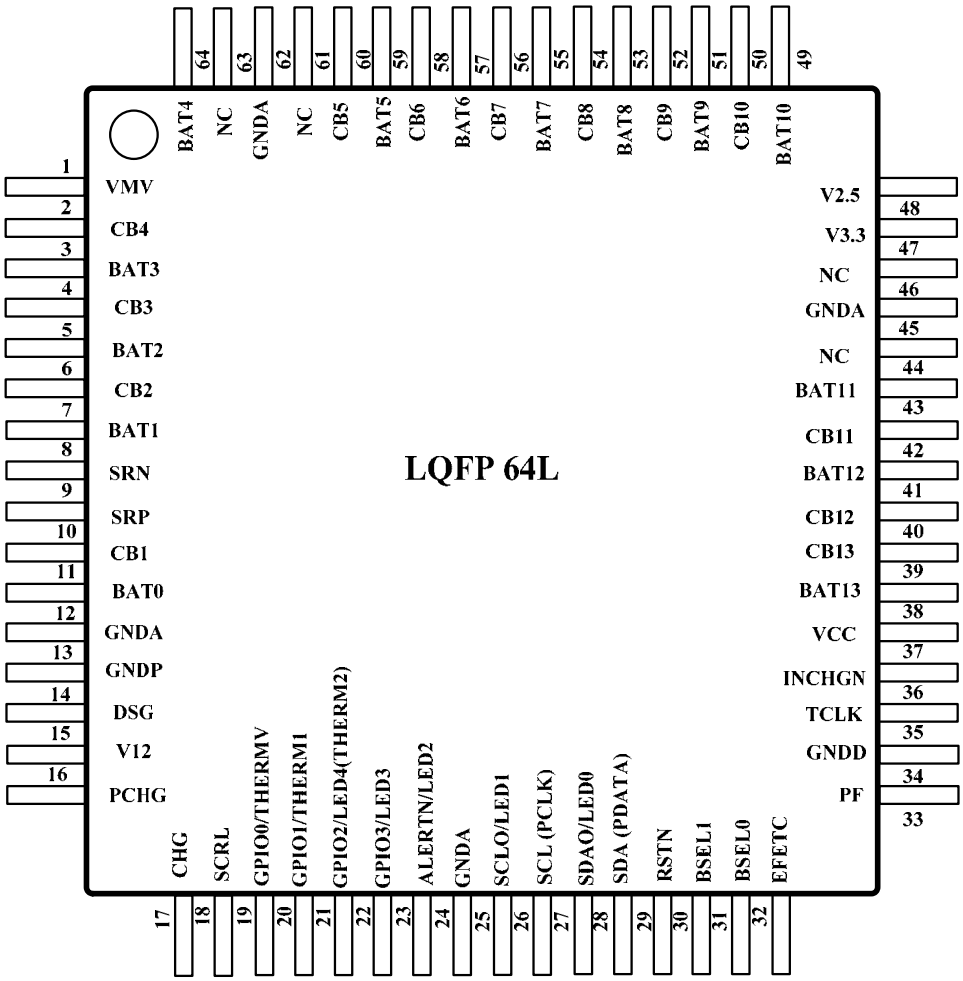
Part Number	Temp Range	Package
OZ890TN	-40°C to 85°C	LQFP64L
OZ890HTN	-40°C to 85°C	LQFP64L

Note: For part selection, refer to the Current Measurement section of Electrical Characteristics on page 12

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
VMV	1	Power	Supply Power for chip; for internal use only	
CB4	2	O	Cell4 external bleeding control	
BAT3	3	I	Cell3 positive input	
CB3	4	O	Cell3 external bleeding control	
BAT2	5	I	Cell2 positive input.	
CB2	6	O	Cell2 external bleeding control	
BAT1	7	I	Cell1 positive input	
SRN	8	I	Current sense resistor negative terminal	
SRP	9	I	Current sense resistor positive terminal	
CB1	10	O	Cell1 external bleeding control	
BAT0	11	I	Cell1 negative input	
GNDA	12	Ground	Analog ground	
GNDP	13	Ground	Power ground	
DSG	14	O	Discharge MOSFET control. Push-pull structure, drive to high level 12V to turn on the discharge MOSFET, drive to low level 0V to turn off the discharge MOSFET.	
V12	15	Power	12V power for discharge MOSFET driver. Maximum supply 10mA in Full Power Mode and Idle Mode, maximum supply is about 100uA in Sleep mode, V12 is disabled in Shut Down mode	
PCHG	16	O	Pre-charge MOSFET control. Sink 5uA current at PCHG MOSFET ON, high impedance at PCHG MOSFET OFF	
CHG	17	O	Charge power MOSFET control. Sink 5uA current at CHG MOSFET ON, high impedance at CHG MOSFET OFF	
SCRL	18	I	Short circuit external release input. It can also be used to detect SC event in sleep mode, and the SC detection threshold is about 1V	
THERMV/ GPIO0	19	I/O	Pin to provide voltage for external thermal sensor	GPIO0 or Pin to provide voltage for external thermal sensor
THERM1/GPIO1	20	I/O	External thermal sensor input 1	GPIO1 or optional external thermal sensor input 1
LED4 (THERM2) /GPIO2	21	I/O	LED driver or optional external thermal sensor input 2	GPIO2 or optional external thermal sensor input 2
LED3/GPIO3 (THERM3)	22	I/O	LED driver	GPIO3 or optional external thermal sensor input 3
LED2/ALERTN	23	O	LED driver	Alert output to Microprocessor (active low) (Open-Drain)
GNDA	24	Ground	Analog ground	
LED1/SCLO	25	I/O	LED driver	4-wire I2C clock output(Open-Drain)

In Hardware Mode, if 2 external thermal sensors are chosen, LED4 will be replaced by THERM2

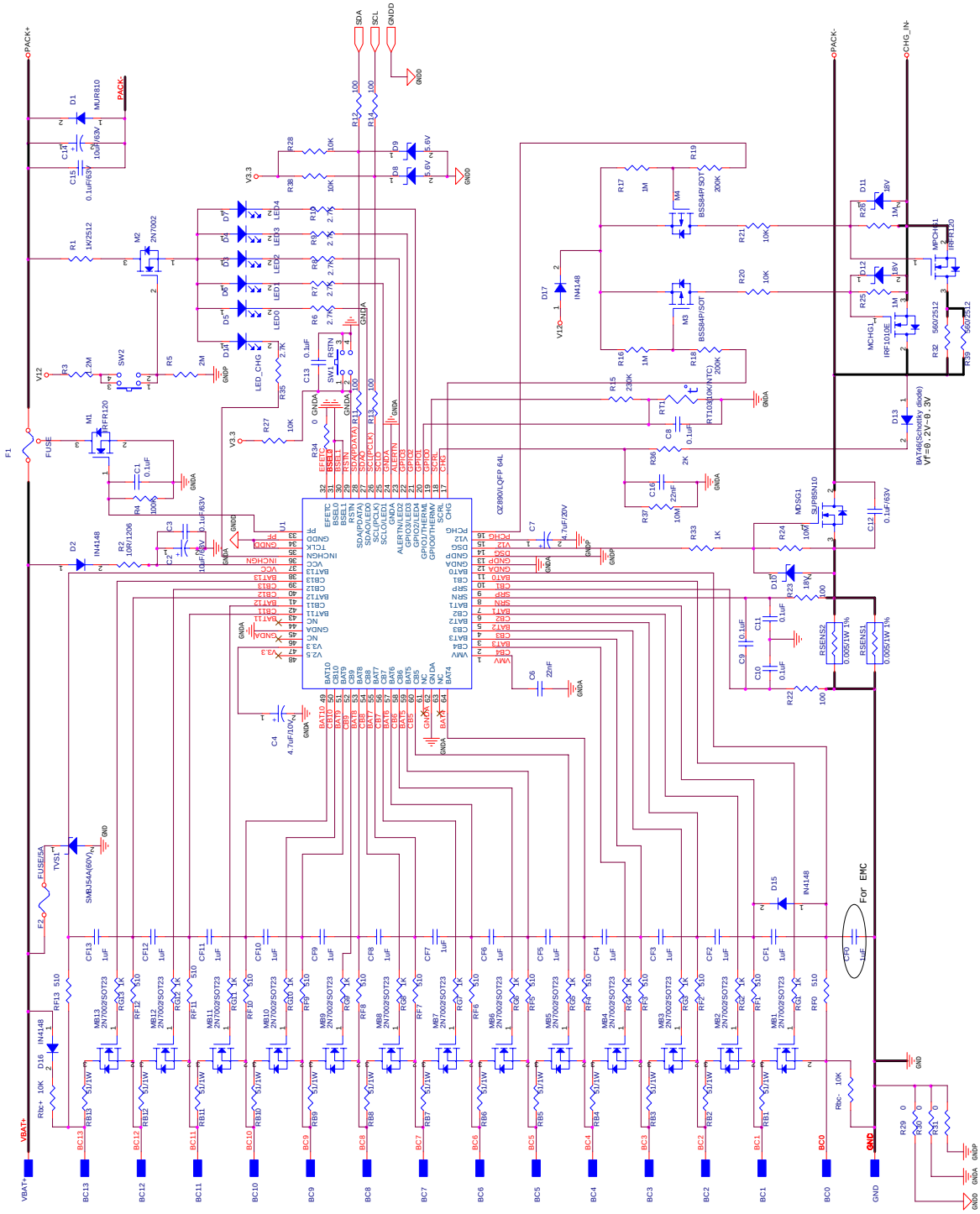
Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
SCL (PCLK)	26	I/O	I2C / PBUS clock line	I2C / PBUS clock line or 4-wire I2C clock input
LED0/SDAO	27	I/O	LED driver	4-wire I2C data output(Open-Drain)
SDA (PDATA)	28	I/O	I2C / PBUS data line	I2C / PBUS data line or 4-wire I2C data input
RSTN	29	I/O	External reset input (active low)	External reset input / Deadman reset output (active low)
BSEL1	30	I	Bus type configuration input1	
BSEL0	31	I	Bus type configuration input0	
EFETC	32	I/O	External MOSFET control signal; it can be configured to input or output through setting EEPROM register	
PF	33	O	Permanent failure output. Active high	
GNDD	34	Ground	Digital ground	
TCLK	35	I	External clock input	
INCHGN	36	O	Indicates “In charge” state. Active low (Open-Drain)	
VCC	37	Power	Chip Power supply	
BAT13	38	I	Cell13 positive input	
CB13	39	O	Cell13 external bleeding control	
CB12	40	O	Cell12 external bleeding control	
BAT12	41	I	Cell12 positive input	
CB11	42	O	Cell11 external bleeding control	
BAT11	43	I	Cell11 positive input	
NC	44		Not connected	
GNDA	45	Ground	Analog ground	
NC	46		Not connected	
V3.3	47	Power	3.3V Power Supply. Maximum supply is 30mA in Full Power Mode and Idle Mode, maximum supply is about 100uA in Sleep Mode and Shut Down Mode	
V2.5	48	Power	Disabled	2.5V Power Supply. Maximum supply is 25mA in Full Power Mode and Idle Mode, maximum supply is about 100uA in Sleep Mode and Shut Down Mode
BAT10	49	I	Cell10 positive input	
CB10	50	O	Cell10 external bleeding control	
BAT9	51	I	Cell9 positive input	
CB9	52	O	Cell9 external bleeding control	
BAT8	53	I	Cell8 positive input	
CB8	54	O	Cell8 external bleeding control	

Name	Pin No	I/O	Description	
			Hardware Mode	Software Mode
BAT7	55	I	Cell7 positive input	
CB7	56	O	Cell7 external bleeding control	
BAT6	57	I	Cell6 positive input	
CB6	58	O	Cell6 external bleeding control	
BAT5	59	I	Cell5 positive input	
CB5	60	O	Cell5 external bleeding control	
NC	61		Not connected	
GNDA	62	Ground	Analog ground	
NC	63		Not connected	
BAT4	64	I	Cell4 positive input	

Note: *All GPIO or open drain pins need to be pulled-high or pulled-low when not used.*

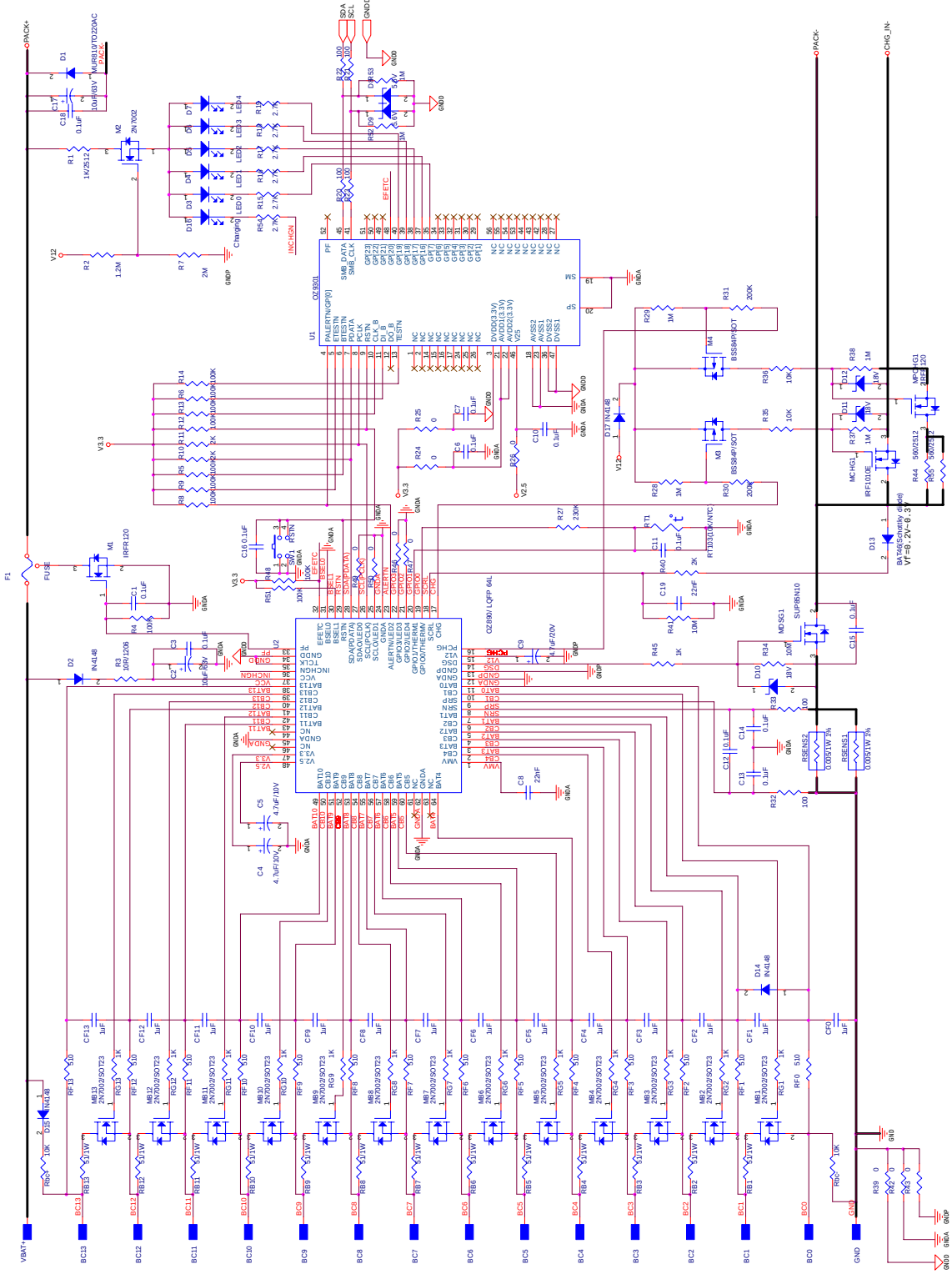
TYPICAL APPLICATION SCHEMATICS

Hardware Mode



Note: *The Application Note "OZ890 AN-11: Application circuits for 5~13 cells Li-ion battery pack" describes the typical application circuits for 5S, 6S, 7S, 8S, 9S, 10S, 11S, 12S and 13S cells Li-Ion battery pack.*

Software Mode



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

Supply voltage range		VCC	-0.5V to 60V
Input	Analog	SRP, SRN	-0.5V to 3.3V
	Analog	THERMV, THERM1, THERM2, THERM3	-0.5V to 6V
	Analog	BATn to BATn-1, n=1 to13	-0.5V to 6V
	Analog	SCRL	-0.5V to 60V
	Analog	VMV	-0.5V to 20V
	Digital	BSEL0, BSEL1	-0.5V to 6V
	Digital	RSTN, TCLK	-0.5V to 6V
Output	Analog	PCHG, CHG	-0.5V to 60V
	Analog	DSG	-0.5V to 12V
	Digital	PF, INCHGN, ALERTN	-0.5V to 6V
	Digital	CBn, n=1 to 13	V_{BATn-1}-0.5V to V_{BATn}
I/O	Digital	GPIO[0:3]/LEDx, SCLO, SCL(PCLK), SDAO, SDA(PDATA), EFETC	-0.5V to 6V
ESD tolerance		Human Body Model (HBM)	2kV
T_{STG}		Storage temperature range	-55°C to 150°C
T_{SOLDER}		Lead temperature (soldering, 10 sec)	300°C

Note 1: *All voltages are with respect to ground of this device except V_{BATn}-V_{BATn-1}, where V_{BATn} denotes the voltage at the pin BATn and n=1 to 13.*

Note 2: *CBn pin voltage must be limited between V_{BATn-1}-0.5V and V_{BATn}, where V_{BATn} denotes the voltage at the pin BATn and n=1 to 13.*

Note 3: *Ground refers to common node of GNDA, GNDD, and GNDP.*

Note 4: *Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

DISSIPATION RATINGS

PACKAGE	T_A≤25°C POWER RATING	DERATING FACTOR ABOVE T_A≥70°C	T_A=85°C POWER RATING	T_A=100°C POWER RATING
LQFP64L	1223 mW	18.27 mW/°C	732 mW	458 mW

RECOMMENDED OPERATING CONDITIONS

Parameter		MIN	NOM	MAX	UNIT
VCC	Supply voltage	8.5		56	V
C_{REG1}	External 3.3-V regulator capacitor	2.2			µF
C_{REG2}	External 2.5-V regulator capacitor	2.2			µF
C_{REG3}	External 12-V regulator capacitor	2.2			µF
I_{REGOUT}	I(REG1+REG2)			30	mA
R_F	Series input resistor at the BATn pin, n=1 to13		510		Ω
C_F	Input filter capacitor at the BATn pin, n=1 to 13		1		µF
f_{I2C}	I^2C Bus Operating Frequency		100		kHz
T_{OPR}	Operating free-air temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

The test conditions are Vcc=36V, T_A=25°C, 85°C respectively; and all time units are based on the internal 512kHz oscillator and have a ±10% tolerance (unless otherwise noted)

Power Supply						
Parameter	**Test Conditions**		**MIN**	**TYP**	**MAX**	**Unit**
I_{VCC} (Supply Current at the VCC pin)	Full Power Mode	Vcc=56V			1500	µA
	Idle Mode				150 (see ***Note 1***)	µA
	Sleep Mode				50	µA
	Shut Down Mode			20	30	µA

Note 1: *During the period when ADC scan is stopped.*

General Purpose Inputs and Outputs (GPIO)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
V_{IH} High-level Input Voltage		2			V
V_{IL} Low-level Input Voltage				0.8	V
V_{OH} Output Voltage High	I_{load} = -0.5mA	V3.3 -0.7			V
V_{OL} Output Voltage Low	I_{load} = 0.5mA			0.4	V
GPIO0 Current Drive Capability			1		mA
GPIO1, GPIO2 and GPIO3 Current Drive Capability			8		mA

Note: *All GPIO pins need to be pulled-high or pulled-low when not used.*

3.3V LDO Regulator $C_{(REG)}$=4.7uF					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage (See ***Note 1***)	I_{load}<25mA, 10V<Vcc<56V	2.97	3.3	3.63	V
Line Regulation (See ***Note 1***)	I_{load}=10mA, 10V<Vcc<56V		10	30	mV
Load Regulation (See ***Note 1***)	0.2mA<I_{load}<25mA Vcc=52V		40	100	mV
3.3V Current Limit (See ***Note 1***)	10V<Vcc<56V			30	mA
Regulator Output Voltage (In Sleep Mode and Shut Down Mode)	I_{load}<100uA, 10V<Vcc<56V	2.8	3.05		V
Current Limit (In Sleep Mode and Shut Down Mode)	10V<Vcc<56V			100	µA

Note 1: In Full Power Mode and Idle Mode

2.5V LDO Regulator $C_{(REG)}$=4.7uF					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Regulator Output Voltage (See ***Note 1***)	I_{load}<20mA, 10V<Vcc<56V,	2.25	2.5	2.75	V

Line Regulation (See ***Note 1***)	I_{load}=5mA, 10V<Vcc<56V		10	30	mV
Load Regulation (See ***Note 1***)	0.2mA<I_{load}<10mA Vcc=52V		40	100	mV
2.5V Current Limit (See ***Note 1***)	10V<Vcc<56V			25	mA
Regulator Output Voltage (In Sleep Mode and Shut Down Mode)	I_{load}<100uA, 10V<Vcc<56V	2.25	2.35		V
Current Limit (In Sleep Mode and Shut Down Mode)	10V<Vcc<56V			100	µA

Note 1: In Full Power Mode and Idle Mode

12V Power

$C_{(REG)}$=4.7uF

Parameter	Test Conditions	MIN	TYP	MAX	Unit
Regulator Output Voltage (See ***Note 1***)	I_{load}<10mA, 15V<Vcc<56V,	9	11	13	V
Line Regulation (See ***Note 1***)	I_{load}=5mA, 15V<Vcc<56V		100	300	mV
Load Regulation (See ***Note 1***)	0.2mA<I_{load}<10mA, Vcc=52V		100	400	mV
12V Current Limit (See ***Note 1***)	15V<Vcc<56V			10	mA
Regulator Output Voltage (In Sleep Mode)	I_{load}<100uA, 15V<Vcc<56V	8.0	9.5		V
Current Limit (In Sleep Mode)	15V<Vcc<56V			100	µA
In Shut Down mode			Off		

Note 1: In Full Power Mode and Idle Mode

Current Measurement

Parameter	Test Conditions		MIN	TYP	MAX	Unit
ADC Input Voltage Range	8.5V<Vcc<56V,		-250		+250	mV
ADC Resolution				16		bit
ADC Conversion Time				256		ms
Accuracy	-10mV<V_{in} <10mV	OZ890TN			±0.5 (see ***Note 1***)	mV
		OZ890HTN			±0.3 (see ***Note 1***)	mV
	V_{in}<-10mV or V_{in}>10mV				±2.5% (see ***Note 1***)	

Note 1: *The accuracy is based on the 1st and 2nd offset cancellation. In software mode, slope calibration can be done to get higher accuracy. Please refer to "OZ890 AN-18: OZ890 Current Measurement Resolution and Accuracy" for detail.*

Cell Voltage Measurement

Parameter		Test Conditions	MIN	TYP	MAX	Unit
Lion-ion Cell Voltage Channel	ADC Input Voltage Range		-0.3		5.0	V
	ADC Resolution			13		bit

	ADC Conversion Time			32		ms
	Accuracy	0.1V<Vin<5V			±0.6% (see ***Note 1***)	
NiMH Cell Voltage Channel	ADC Input Voltage Range		0.1		5.0	V
	ADC Resolution			13		bit
	ADC Conversion Time			32		ms
	Accuracy	0.1V<Vin<5V			±0.6% (see ***Note 1***)	

Note 1: *The accuracy is based on the 1st and 2nd offset cancellation. In software mode, slope calibration can be done to obtain higher accuracy. Please refer to "OZ890 AN-19: Resolution and Accuracy of OZ890 Cell Voltage and Temperature Measurement and accuracy of OC/SC Protection" for detailed description.*

Temperature and GPIO Channel Measurement						
Parameter		**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Internal Temperature (1 channel)	ADC Input Voltage Range		0.1		2.5	V
	ADC Resolution			13		bit
	ADC Conversion Time			32		ms
	Accuracy	0.1V<Vin<2.5V			±0.5% (see ***Note 1***)	
GPIO[1:2] channel	ADC Input Voltage Range		0.1		2.5	V
	ADC Resolution			13		bit
	ADC Conversion Time			32		ms
	Accuracy	0.1V<Vin<2.5V			±0.5% (see ***Note 1***)	
GPIO[3]	ADC Input Voltage Range		0.1		2.5	V
	ADC Resolution		13		16	bit
	ADC Conversion Time	13 bits resolution		32		ms
		16 bits resolution		256		
	Accuracy	0.1V<Vin<2.5V			±0.5% (see ***Note 1***)	

Note 1: *The accuracy is based on the 1st and 2nd offset cancellation. In software mode, slope calibration can be done to get higher accuracy. Please refer to "OZ890 AN-19: Resolution and Accuracy of OZ890 Cell Voltage and Temperature Measurement and accuracy of OC/SC Protection" for detailed description.*

Over-Current (OC) And Short-Circuit (SC) Protection					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
Charge OC Detection Threshold (5-bit setup)		10		105	mV
Discharge OC Detection Threshold (6-bit setup)		-285		-30	mV
OC Detection Threshold Step		5			mV

Charge OC Hysteresis Value		N/A			
Discharge OC Hysteresis Value		10			mV
OC Protection Delay Time (8-bit setup)		2		16300	ms (see ***Note 1***)
Charge OC Release Delay Time (4-bit setup)		1		31	S (see ***Note 1***)
Discharge OC Release Delay Time (4-bit setup)		1		31	S (see ***Note 1***)
OC Release Delay Time Step		Variable			
OC Detection Threshold accuracy			±3.5 (see ***Note 2***)		mV
SC Detection Threshold (6-bit setup)		-620		-50	mV
SC Detection Threshold Step		-10			mV
SC Hysteresis Value		20			mV
SC Protection Delay Time (8-bit setup)		8		32800	us (see ***Note 3***)
SC Release Delay Time (4-bit setup)		0.25		1.75	min
SC Release Delay Time Step		0.25min			
SC Detection Threshold accuracy			±10 (see ***Note 2***)		mV
SC Detection Threshold in Sleep Mode by SCRL pin		0.8	1	1.2	V

Note 1: *8-bit OC delay control byte divided into two sections, The high 5 bits are used to indicate the over current delay time as N+1 (N is the 5 bits value) delay units; ATE tested OC protection delay time in digital pattern test mode. The low 3 bits are used to indicate the OC delay unit as follows:*

OC delay scale	OC delay unit	OC delay scale	OC delay unit
3'b000	2ms*1=2ms	3'b100	2ms*31=62ms
3'b001	2ms*3=6ms	3'b101	2ms*63=126ms
3'b010	2ms*7=14ms	3'b110	2ms*127=254ms
3'b011	2ms*15=30ms	3'b111	2ms*255=510ms

The OC delay time = (N+1)*(OC delay unit), so its range is 2ms~16.3s

Note 2: *After offset cancellation.*

Note 3: *8-bit SC delay control byte divided into two sections. The high 5 bits are used to indicate the short circuit delay time as N+1 (N is the 5 bits value) delay units; the low 3 bits are used to indicate the SC delay unit as follows:*

SC delay scale	SC delay unit	SC delay scale	SC delay unit
3'b000	4us*2=8us	3'b100	4us*32=128us
3'b001	4us*4=16us	3'b101	4us*64=256us
3'b010	4us*8=32us	3'b110	4us*128=512us
3'b011	4us*16=64us	3'b111	4us*256=1024us

The SC delay time = (N+1)*(SC delay unit), so its range is 8us~32.8ms

Over-Voltage (OV) And Under-Voltage (UV) Protection					
Parameter	**Test Condition**	**MIN**	**TYP**	**MAX**	**Unit**
OV Detection Threshold		13bits programmable (0-5V)			
OV Release Value		13bits programmable (0-5V)			
OV Detection Threshold Accuracy		See ***Note 1***			
UV Detection Threshold		13bits programmable (0-5V)			
UV Release Value		13bits programmable (0-5V)			
UV Detection Threshold Accuracy		See ***Note 1***			
OV/UV Protection Delay Time (4-bit setup)		1		16	S (See note 2)
OV/UV Protection Delay Time Step		1			S (See note 2)
OV/UV Release Delay Time		same as OV/UV protection delay time			
OV/UV Release Delay Time Step		same as OV/UV protection delay time step			

Note 1: *Determined by cell voltage measurement accuracy.*
Note 2: ATE tested OV/UV protection delay time in digital pattern test mode.

Permanent Failure Protection (VLPF, VHPF, CUPF and MFPF)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
VLPF Threshold		13bits programmable (0-5V)			
VLPF Detection Threshold Accuracy		See ***Note 1***			
VHPF Threshold		13bits programmable (0-5V)			
VHPF Detection Threshold Accuracy		See ***Note 1***			
CUPF threshold		13bits programmable(0-5V)			
CUPF Detection Threshold Accuracy		See ***Note 1***			
MFPF Detection Threshold		See ***Note 2***			
PF delay time (4-bit setup)		2		32	S (See note 3)
PF delay time step		2			S (See note 3)

Note 1: *Determined by cell voltage measurement accuracy.*
Note 2: *When the charge and Pre-charge Power MOSFETs are both off but some current still flows into the battery pack and its value is larger than the charge state threshold, or when the discharge Power MOSFET is off but some current still flows out of the battery pack and its value is less than the discharge state threshold, MOSFET failure is detected.*
Note 3: ATE tested PF delay time in digital pattern test mode

Internal Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
OT Detection Threshold		13bits Programmable (0-2.5V)			(see ***Note 1***)
OT Detection release Value		13bits Programmable (0-2.5V)			(see ***Note 1***)

UT Detection Threshold		13bits Programmable (0-2.5V)			(see ***Note 1***)
UT Detection Release Value		13bits Programmable (0-2.5V)			(see ***Note 1***)
OT/UT Protection Delay Time (4-bit setup)		1		16	TSP (see ***Note 2***)
OT/UT Protection Delay Time Step		1			TSP (see ***Note 2***)
OT/UT Release Delay Time		same as OT/UT protection delay time			
OT/UT Release Delay Time Step		same as OT/UT protection delay time step			

Note 1: *According to the internal temperature sensor's characteristics, every 2.1mV in voltage corresponds to 1℃ in temperature.*
Note 2: *TSP = Temperature Scan Period for all Temperature Channel. Please refer to the section "Time Slot in Different Configuration".*

External Thermal Protection (OT & UT)					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit/Step**
OT Detection Threshold		13bits Programmable (0-2.5V)			(see ***Note 1***)
OT Detection release Value		13bits Programmable (0-2.5V)			(see ***Note 1***)
UT Detection Threshold		13bits Programmable (0-2.5V)			(see ***Note 1***)
UT Detection Release Value		13bits Programmable (0-2.5V)			(see ***Note 1***)
OT/UT Protection Delay Time		same as OT/UT delay time for internal thermal protection			
OT/UT Protection Delay Time Step		same as OT/UT delay time step for internal thermal protection			
OT/UT Release Delay Time		same as OT/UT protection delay time			
OT/UT Release Delay Time Step		same as OT/UT protection delay time step			

Note 1: *Depends on external temperature sensor characteristics.*

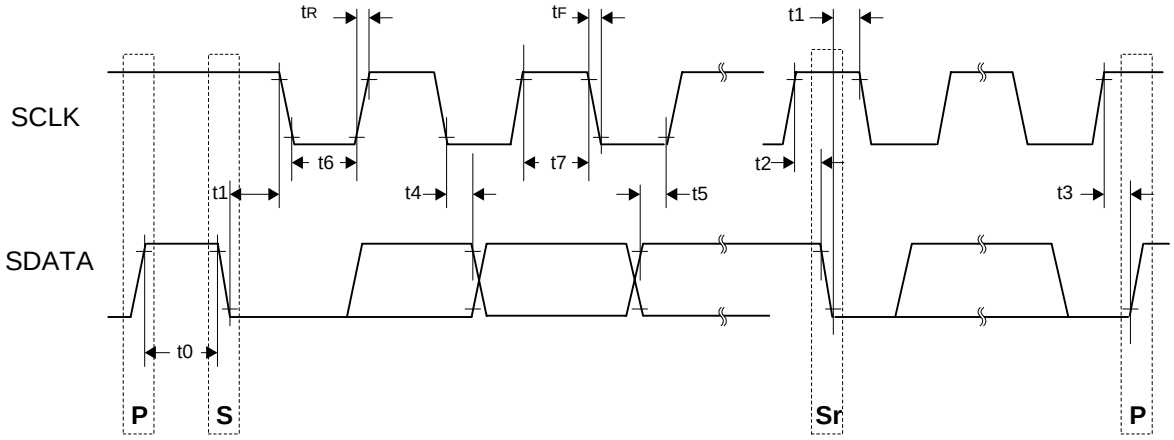
Power MOSFET Driver Circuit					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
CHG on, sink current (constant current source),	Vcc=56V		5	7	μA
CHG off, high impedance	Vcc=56V		0	0.9	μA
PCHG on, sink current (constant current source)	Vcc=56V		5	7	μA
PCHG off, high impedance	Vcc=56V		0	0.9	μA
DSG High Level	Vcc=56V		11	13	V
DSG Low Level	Vcc=56V			0.5	V
PWM Discharge Frequency	Vcc=56V			8	kHz

Internal Oscillator					
Parameter	**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**

512kHz Oscillator Frequency	Vcc=56V,	470	512	552	KHz
32kHz Oscillator Frequency	Vcc=56V	20	30	42	KHz

AC TIMING

I²C Bus Timing



Symbol	Parameter	Limits		Units	Note
		Min	Max		
f_{I2C}	I^2C Bus Operating Frequency	10	400	kHz	
t_0	Bus free time between Stop and Start condition	1.3	-	µs	
t_1	Hold time after (Repeated) Start condition. After this period, the first clock is generated	0.6	-	µs	
t_2	Repeated Start condition set up time	0.6	--	µs	
t_3	Stop Condition setup time	0.6	-	µs	
t_4	Data hold time	150	-	ns	
t_5	Data setup time	100	-	ns	
t_6	Clock low period	1.3	-	µs	
t_7	Clock high period	0.6		µs	
t_F	Clock/Data Fall time	-	300	ns	See ***Note 1***
t_R	Clock/Data Rise Time	-	300	ns	See ***Note 1***

Note 1: *Rise Time and Fall Time are measured between 10% and 90% of the signal amplitude.*

FUNCTIONAL DESCRIPTION

OZ890 Power-Up Sequence

Fig.1 shows the OZ890 power up sequence. When power supply is applied to VCC>8.5V and the voltage at pin BAT4 of OZ890 is higher than 6.5V, the common bias starts first, followed by the band-gap and 3.3V & 2.5V LDOs. When V3.3>2.4V, the power on reset block generates POR signal to enable the 512K oscillator and initializes the digital section. When power and clock are ready, the digital circuits will read the pin configuration and EEPROM data, which in turn determines the working state.

If RSTN_BYPASS (bit5 of EEPROM register 32h) is “0” (default value), OZ890 will go to the assembly state. In this state, OZ890 does not do ADC safety scan; only after pin RSTN (pin 29) negative pulse (low active reset signal), OZ890 can go to the normal working state. If RSTN_BYPASS is “1”, OZ890 will go to the normal working state directly.

When the voltage at pin BAT4 of OZ890 is lower than 6.5V or VCC is lower than 8.5V, OZ890 is in shutdown status. All LDOs (V3.3 and V12) are disabled and all MOSFETs are disabled.

There is one essential requirement of assembly sequence while connecting the battery cells to the protection board using OZ890. In general, the ground pins and VCC pin of OZ890 should get power before any other pins. Please refer to the Application Note "***OZ890 AN-1: Battery Pack Assembly Sequence and Connections Technique***" for details.

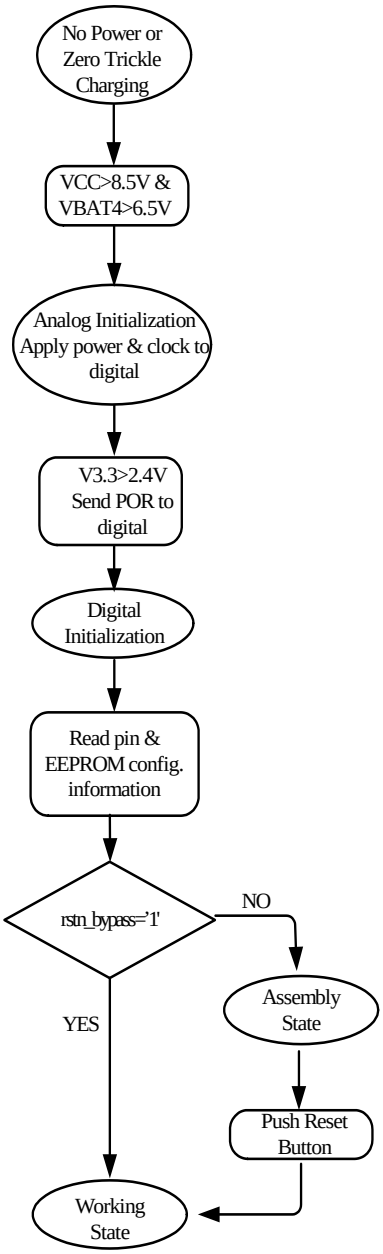


Fig.1 OZ890 power up sequence

Hardware Mode and Software Mode

OZ890 supports two operation modes, the Hardware mode and Software mode. The mode of operation is selected by setting the configurable parameter HM (bit0 in EEPROM register 32h). If it is set to “1”, OZ890 works in Hardware Mode; if set to “0”, OZ890 works in Software Mode. In Hardware Mode, all controls are handled in OZ890 chip; in Software Mode, the software has some flexibility to control OZ890. The differences between Hardware Mode and Software Mode are summarized in the following table.

Feature		Hardware Mode	Software Mode
Pin Function	THERMV/GPIO0	External thermal sensor driver voltage	GPIO0 or External thermal sensor driver voltage
	THERM1/GPIO1	External thermal sensor input 1	GPIO1or External thermal sensor input 1
	LED4 (THERM2)/GPIO2	LED driver or optional external thermal sensor input 2	GPIO2 or optional external thermal sensor input 2
	LED3/GPIO3 (THERM3)	LED driver	GPIO3 or optional external thermal sensor input 3
	LED2/ALERTN	LED driver	Alert output to Microprocessor (active low) (Open-Drain)
	LED1/SCLO	LED driver	4-wire I2C clock output (Open-Drain)
	SCL (PCLK)	I2C/PBUS clock line	I2C/PBUS clock line or 4-wire I2C clock input
	LED0/SDAO	LED driver	4-wire I2C data output (Open-Drain)
	SDA (PDATA)	I2C/PBUS data line	I2C/PBUS data line or 4-wire I2C data input
	RSTN	External reset input	External reset input/Deadman reset output
	V2.5	Disabled	2.5V Power Supply. Maximum supply is 25mA in full power mode, maximum supply is about 100uA in sleep mode and shut down mode
ADC Measurement	ADC Scan Period	In Full Power Mode, it is 1s; in Idle Mode, by setting EEPROM Register 27h, bit[6:4], it can be set to 1s, 8s, 16s, 24s, 32s, 40s, 48s or 56s.	It can be set to 1s, 8s, 16s, 24s, 32s, 40s, 48s or 56s by writing Operation Register 07h, bit[6:4].
	ADC Channel	• Only GPIO1 and GPIO2 can be used as temperature channel • GPIO3 cannot be used as a special ADC channel • No time slot for Microprocessor request ADC	• GPIO1, GPIO2 and GPIO3 can be used as temperature channel • GPIO3 can be used as a special ADC channel • The Microprocessor can do request ADC to the specified channel in a reserved time slot by accessing Operation Register 24h and 25h.
	Offset Calibration	Auto done by OZ890	Must be executed by Microprocessor
Voltage Based Gas Gauge		Enabled	Disabled
Internal/External Bleeding		• Can be done in charge state or idle state by hardware engine	• Must be controlled by Microprocessor
Battery Protection and Release		• Battery protection and release are fully controlled by Battery Protection Engine in OZ890 • No error alarm by the ALERTN pin • Deadman PF function is disabled • When cell unbalance or MOSFET failure is detected and persists for the PF delay time, CUPF or MFPF will occur	• Protection actions are controlled by Battery Protection Engine of OZ890. OZ890 can issue the protection alarm by the ALERTN pin to inform. Microprocessor. • For release action, they are fully controlled by Microprocessor through accessing Operation Register 1fh. • Deadman PF function is enabled • When cell unbalance or MOSFET failure is detected, the ALERTN pin will be active to inform the Microprocessor which will make decision. • Microprocessor can provide other software level protections and control MOSFETs (ON/OFF) by assessing Operation Register 1Eh directly.

Power Mode	• 4 Power Modes: Full Power Mode, Idle Mode, Sleep Mode, Shut Down Mode • OZ890 is self-directed in transition from Full Power Mode/Idle Mode to Sleep Mode	• 3 Power Modes: Full Power Mode, Sleep Mode, Shut Down Mode • OZ890 must receive the sleep request from the external Microprocessor in transition from Full Power Mode to Sleep Mode
Serial Communication Bus	Only 2-wire I2C Bus function	2-wire or 4-wire I2C Bus function

Measurements

OZ890 includes a multi-channel ADC (as shown in Fig. 2) for current, voltage and temperature measurement. OZ890's multi-channel ADC measures up to 13 cell voltages, current, internal temperature and external temperature based on cyclic scan and time slot method. It will periodically measure all these values by predefined scan period which is listed as below.

- In Hardware Mode
  - In Full Power Mode, it is 1s.
  - In Idle Mode, it can be selected among 1s, 8s, 16s, 24s, 32s, 40s, 48s and 56s by setting SCN_RT2 - SCN_RT0 in EEPROM (bits [6:4] of EEPROM Register 27h).
- In Software Mode
  - It can be selected among 1s, 8s, 16s, 24s, 32s, 40s, 48s and 56s by setting SCN_RT2 - SCN_RT0 in Operation Register (bits [6:4] of Operation Register 07h). There is no Idle Mode concept in Software Mode.

When OZ890 goes into Sleep Mode or Shut Down Mode, the ADC scan will be stopped.

During one measurement period, voltage, current, etc will be measured one by one in different time slot.

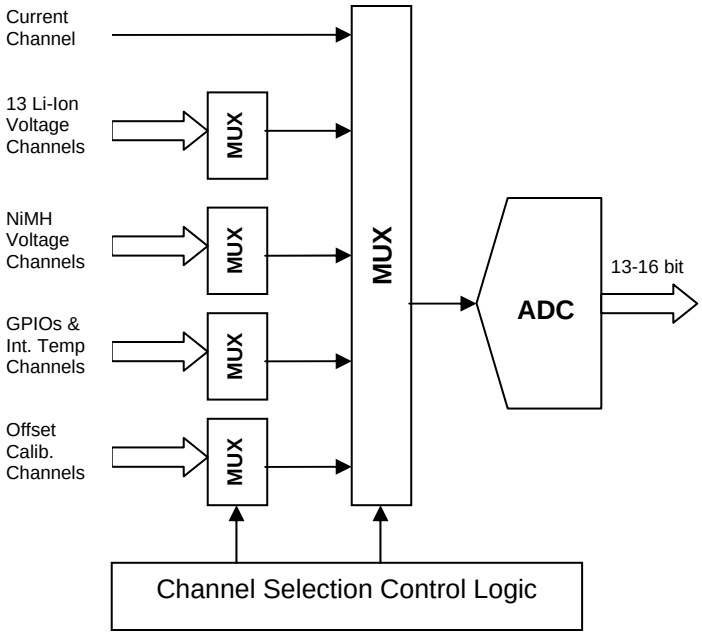


Fig. 2, Muti-Channel ADC

ADC Channel Description

Current Channel (1 channel)
This is a dedicated channel to measure the current across the sense resistor during charging and discharging for coulomb counting or other purpose.

Resolution: 16-bit (signed)
Input Voltage Range: ± 250mV
Auto offset cancellation

Since OZ890 uses a 16-bit (with sign bit) ADC for current measurement with resolution of 15 bits positive; 15 bits negative, the Least Significant Bit (LSB) ADC resolution is $250mV/2^{15}$=7.6μV. But in practice it is not equal to the current measurement accuracy because of ADC offset and slope error and other application error factors. Please refer to the application note "***OZ890 AN-18: OZ890 Current Measurement Resolution and Accuracy***" for detailed current accuracy information and how to acquire high current measurement accuracy.

The sense resistor value needs to be selected based on the normal working current range in the real application (EEPROM register 34h is used to store the sense resistor value). The higher the sense resistor used, the higher the voltage drop is across the sense resistor. Higher sense resistor values will result in better accuracy when measuring small current signals.

Slope calibration can be implemented in Software Mode for better accuracy. Please refer to the application note "***OZ890 AN-8: How to Do ADC Calibration***" for details.

Li-Ion Cell Voltage Channel (5~13 channels)
These channels are designed for cell voltage measurement.

Resolution: 13bits (signed)
Input Voltage Range: -0.3V~5.0V
Auto offset cancellation

Since OZ890 uses a 13-bit (with sign bit) ADC for cell voltage measurement with resolution of 12 bits positive; 12 bits negative, the Least Significant Bit (LSB) ADC resolution is $5V/2^{12}$ = 1.22mV, but in practice it is not equal to the cell voltage measurement ADC resolution because of ADC offset and slope error and other errors introduced by level shift circuit. Please refer to the application note "***OZ890 AN-19: Resolution and Accuracy of OZ890 Cell Voltage and Temperature Measurement and accuracy of OC/SC Protection***" for details.

Slope calibration can be implemented in Software Mode for better accuracy.

NiMH Cell Voltage Channel (2 channels for 20S, 3 channels for 30S)
For monitoring NiMH battery pack, OZ890 does not scan each cell's voltage; instead it only scans every 10-series NiMH cell total voltage. For 20S NiMH battery pack, 10S tap connects to pin BAT4, the top positive terminal (20S) connects to pin BAT8. For 30S NiMH battery pack, 10S tap connects to pin BAT4, the 20S tap connects to pin BAT8, the top positive terminal (30S) connects to pin BAT12. In order to scale the respective sense point voltage to the ADC input range, OZ890 has 3 internal dividers to scale down the sense point voltage. For the BAT4 point sense voltage, divided by 6.667; for the BAT8 point sense voltage, divided by 13.333; For BAT12 point sense voltage, divided by 20. For 20 series NiMH battery pack, OZ890 only scans the BAT4 and BAT8 voltage channel instead of scanning all the individual cell voltage channels; and also, for 30 series NiMH battery pack, OZ890 only scans the BAT4, BAT8 and BAT12 voltage. Additionally, it can be configured to just sense BAT12 (for 30S) or BAT8 (for 20S) voltage by 1 bit in EEPROM register 26h bit7.

Resolution: 13bits (signed)
Input Voltage Range: 0.1V~5.0V

Auto offset cancellation
Please refer to the application note "***OZ890 AN-19: Resolution and Accuracy of OZ890 Cell Voltage and Temperature Measurement and accuracy of OC/SC Protection***" for detailed resolution.

Slope calibration can be implemented in Software Mode for better accuracy.

Internal Temperature (1 channel)
This channel is designed for internal temperature sensor.

Resolution: 13bits (signed)
Input Voltage Range: 0.1V~2.5V
Auto offset cancellation

Please refer to the application note "***OZ890 AN-19: Resolution and Accuracy of OZ890 Cell Voltage and Temperature Measurement and accuracy of OC/SC Protection***" for detailed resolution.

GPIO Channel (3 channel)
In Hardware Mode, GPIO1 can be configured as external temperature sensor channel; GPIO2 can be configured as external temperature sensor channel or LED4 driver. GPIO3 can be used as LED3 driver only. Please refer to the section "***External Temperature Sensor***" for detailed external temperature sensor configuration.

In Software Mode, GPIO1 can be used as external temperature sensor channel or general purpose I/O by configuring G1_MD1 - G1_MD0 (bit[1:0] of Operation Register 2dh). GPIO2 can be used as external temperature sensor channel or general purpose I/O by configuring G2_MD1 – G2_MD0 (bit[3:2] of Operation Register 2dh). GPIO3 can be used as external temperature sensor channel or general purpose I/O by configuring G3_MD1 – G3_MD0 (bit[7:6] of Operation Register 2dh). It also can be configured as a special ADC channel by setting G3_MD1 – G3_MD0 to 2'b11.

In some applications, Hall Effect device is used to sense current. In this case, OZ890 will use GPIO3 to sense the current instead of the SRP and SRN pins. Besides this, some configurations are also needed for EEPROM and Operation Registers. The steps are as follows:

- G3_MD1 – G3_MD0="11"; (Configure GPIO3 as a special ADC channel)
- G3_RES1 – G3_RES0 (Operation Register 2dh, bit[5:4])="11"; (Configure the ADC resolution as 16bits. Though it also can be configured as 13~15bits, it is always recommended to configure the ADC resolution as 16bits because the obtained value will be compared with the charge state threshold (configurable at bit[7:6] of EEPROM Register 29h) and the discharge state threshold (by setting bit[7:5] of EEPROM Register 28h) to decide the battery pack state).
- NO_SNSR (EEPROM Register 27h, bit7) ="1". (Disable the current ADC channel and make the GPIO3 channel use the time slot for it).

Accuracy: 13bits (signed) for GPIO1 and GPIO2; 13~16bits (signed) for GPIO3
Input Voltage Range: 0.1V~2.5V
Auto offset cancellation

Please refer to the application note "***OZ890 AN-19: Resolution and Accuracy of OZ890 Cell Voltage and Temperature Measurement and accuracy of OC/SC Protection***" for detailed resolution.

Slope calibration can be implemented in Software Mode for better accuracy.

Offset Calibration Channel

In Hardware Mode, the offset calibration will be done automatically once every 30 minutes and the offset values are stored in the corresponding registers, the normal ADC scan will be paused while executing the calibration. There are 5 offset values which are named as Group1 Offset, Group2 Offset, Group3 Offset, GPIO Offset and Current Offset. They can be used to adjust the ADC channels' values as following table:

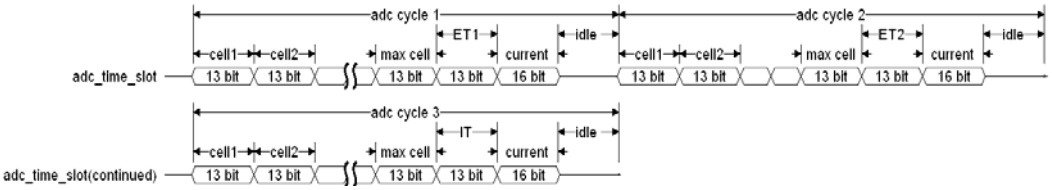
Offset Name	Register Storing the Offset	Voltage Name	Register Storing the Adjusted ADC Value
Group1 Offset	Operation Register 56h	Cell1 voltage	Operation Register 33h, 32h
		Cell2 voltage	Operation Register 35h, 34h
		Cell3 voltage	Operation Register 37h, 36h
		Cell4 voltage	Operation Register 39h, 38h
		Cell5 voltage	Operation Register 3bh, 3ah
Group2 Offset	Operation Register 57h	Cell6 voltage	Operation Register 3dh, 3ch
		Cell7 voltage	Operation Register 3fh, 3eh
		Cell8 voltage	Operation Register 41h, 40h
		Cell9 voltage	Operation Register 43h, 42h
Group3 Offset	Operation Register 58h	Cell10 voltage	Operation Register 45h, 44h
		Cell11 voltage	Operation Register 47h, 46h
		Cell12 voltage	Operation Register 49h, 48h
		Cell13 voltage	Operation Register 4bh, 4ah
GPIO Offset	Operation Register 59h	GPIO1 voltage	Operation Register 4dh, 4ch
		GPIO2 voltage	Operation Register 4fh, 4eh
		GPIO3 voltage	Operation Register 51h, 50h
Current Offset	Operation Register 5ah, 5bh	Current sensor voltage	Operation Register 55h, 54h

In Software Mode, the offset calibration will not be done automatically. But the Microprocessor can request OZ890 to do offset channel ADC in the reserved time slot. In this case, the normal ADC scan would not be paused by the offset calibration. Please refer to the Application Note "***OZ890 AN-6: Software Mode Guide***" for details of the offset calibration in Software Mode.

The above 5 offset values are also named as the 1st offsets which would be updated by auto-calibration mechanism embedded in hardware or software when OZ890 is working. In OZ890, there are the 2nd offsets for cell voltage channels, GPIO channels and current channel. The 2nd offsets are obtained at ATE test stage, stored in EEPROM Register 05h~17h and cannot be modified after the bit "ATE_FRZ" (EEPROM Register 25h, bit7) is set to "1". Considering that battery protection board manufacturers may want to modify the 2nd offsets, O2Micro provides the 2nd offset Board level calibration function and procedure in the software utility and in *"**OZ890 AN-6: Software Mode Guide**"* .

Time Slot in Different Configuration

ADC Time Slots for Li-ion in Hardware Mode



Note:

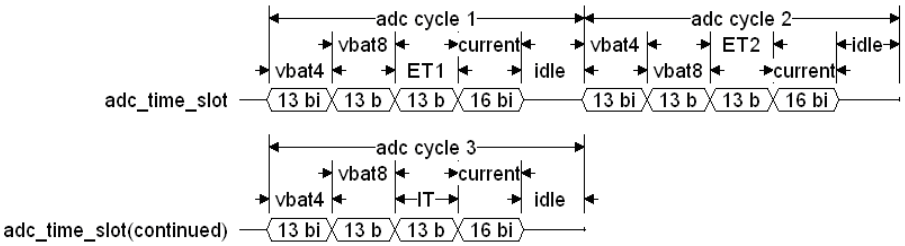
(1) The slot's length is not in scale.

(2) ET1, ET2 indicate the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage.

(3) ET1 and ET2 can be configured to be enabled or disabled independently. If external temperatures ET1 and ET2 are both enabled, adc cycle1, adc cycle2, adc cycle3 will be repeated; if only ET1 is enabled,

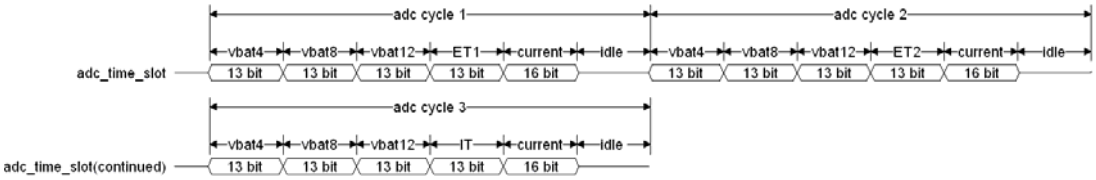
adc cycle1, adc cycle3 will be repeated; if only ET2 is enabled, adc cycle2, adc cycle3 will be repeated; if there is no external temperature, only adc cycle3 will be repeated.

ADC Time Slots for 20S NiMH in Hardware Mode



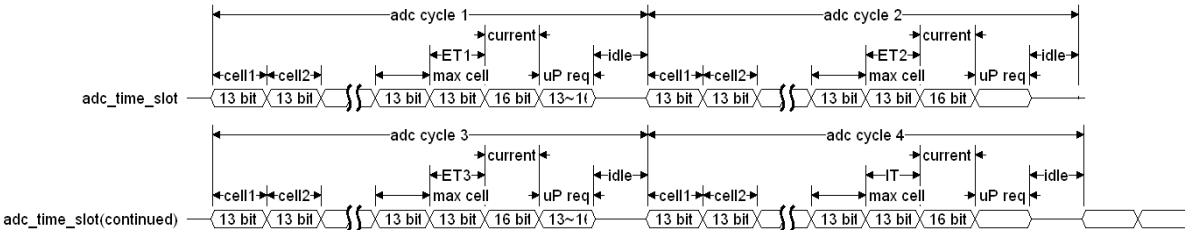
Note:
(1) The slot's length is not in scale.
(2) ET1, ET2 indicate the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage.
(3) The vbat4 is for 10 cells' voltage; the vbat8 is for 20 cells' voltage. If NIMH_VPKOL (EEPROM register 26h, bit7) is 1, there is only vbat8 time slot without vbat4 time slot; if NIMH_VPKOL is 0, there are vbat4, vbat8 time slots.
(4) If external temperature ET1 & ET2 are both enabled, adc cycle1, adc cycle2, adc cycle3 will be repeated; if only ET1 is enabled, adc cycle1, adc cycle3 will be repeated; if only ET2 is enabled, adc cycle2, adc cycle3 will be repeated; if no external temperature is there, only adc cycle3 will be repeated.

ADC Time Slots for 30S NiMH in Hardware Mode



Note:
(1) The slot's length is not in scale.
(2) ET1, ET2 indicates the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor voltage.
(3) The vbat4 is for 10 cells' voltage; the vbat8 is for 20 cells' voltage, the vbat12 is for 30 cells' voltage. If NIMH_VPKOL is 1, there is only vbat12 time slot without vbat4, vbat8 time slot; if NIMH_VPKOL is 0, there are vbat4, vbat8, vbat12 time slots.
(4) If ET1and ET2 external temperature are enabled, adc cycle1, adc cycle2, adc cycle3 will be repeated; If only ET1 external temperature is enabled, adc cycle1, adc cycle3 will be repeated; if only ET2 external temperature is enabled, adc cycle2, adc cycle3 will be repeated; if no external temperature, only adc cycle3 will be repeated.

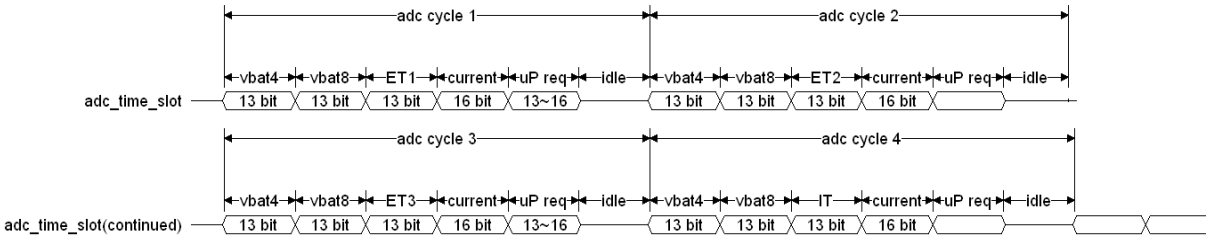
ADC Time Slots for Li-ion in Software Mode



Note:
(1) The slot's length is not in scale.

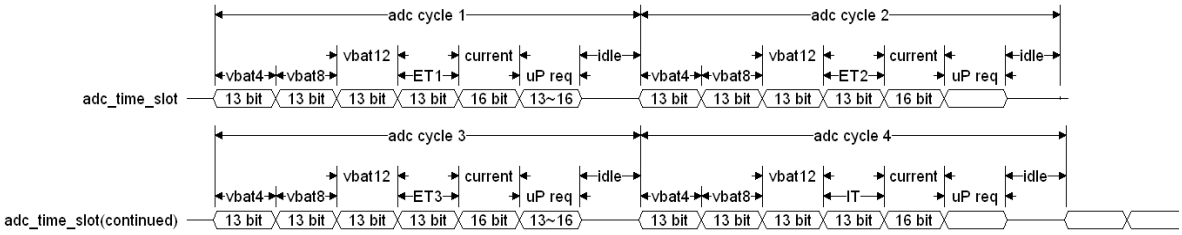
(2) ET1, ET2, ET3 indicates the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor or GPIO3 (When NO_SNSR (Bit 7 in EEPROM register 27h) is "1" and G3_MD1 – G3_MD0 (Bit[7:6] in Operation register 2dh) is "11", GPIO3 can be used as a special ADC channel to detect current in some applications. In this mode, the current sensor channel is disabled and the time slot for it is occupied by the GPIO3 channel).
(3) The "µP req" indicates the ADC request from the Microprocessor which can be 13~16bit. In one ADC cycle, at least one Microprocessor ADC request can be completed. The Microprocessor will not launch new ADC request until the previous ADC request is finished. In OZ890, there is an ADC busy bit (bit0 in Operation Register 25h) to inform the Microprocessor that the ADC request is being processed; also OZ890 will provide ADC event bit (bit6 in Operation Register 2bh) to tell the Microprocessor that the ADC request is completed. The specified ADC request channel and its resolution are set in Operation Register 24h.
(4) If ET1, ET2 and ET3 external temperature are enabled, adc cycle1, adc cycle2, adc cycle3, adc cycle4 will be repeated; if only ET1, ET2 external temperature are enabled, adc cycle1, adc cycle2, adc cylce4 will be repeated; if only ET1 external temperature is enabled, adc cycle1, adc cylcle4 will be repeated; if there is no external temperature, only adc cycle4 will be repeated.

ADC time slots for 20S NiMH in Software Mode



Note:
(1) The slot's length is not in scale.
(2) ET1, ET2, ET3 indicates the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor or GPIO3 (GPIO3 can be used as a special ADC channel to detect current in some applications. In this mode, the current sensor channel is disabled and the time slot for it is occupied by the GPIO3 channel).
(3) The vbat4 is for 10 cells' voltage; the vbat8 is for 20 cells' voltage. If NIMH_VPKOL (EEPROM register 26h, bit7) is 1, there is only vbat8 time slot without vbat4 time slot; if NIMH_VPKOL is 0, there are vbat4, vbat8 time slots.
(4) The "µP req" indicates the ADC request from the Microprocessor which can be 13~16bit. In one ADC cycle, at least one Microprocessor ADC request can be completed. The Microprocessor will not launch new ADC request until the previous ADC request is finished. In OZ890, there is an ADC busy bit (bit0 in Operation Register 25h) to inform the Microprocessor ADC request is being processed; also OZ890 will provide ADC event bit (bit6 in Operation Register 2bh) to tell the Microprocessor that the ADC request is completed. The specified ADC request channel and its resolution are set in Operation Register 24h.
(5) If ET1, ET2, and ET3 external temperature are enabled, adc cycle1, adc cycle2, adc cycle3, adc cycle4 will be repeated; if only ET1and ET2 external temperature are enabled, adc cycle1, adc cycle2, adc cylce4 will be repeated; if only ET1 external temperature is enabled, adc cycle1, adc cylcle4 will be repeated; if there is no external temperature, only adc cycle4 will be repeated.

ADC Time Slots for 30S NiMH in Software Mode



Note:

(1) The slot's length is not to scale.

(2) ET1, ET2, ET3 indicates the external temperature; IT indicates the internal temperature; current indicates the current channel from current sensor or GPIO3 (GPIO3 can be used as a special ADC channel to detect current in some applications. In this mode, the current sensor channel is disabled and the time slot for it is occupied by the GPIO3 channel).

(3) The vbat4 time slot is for 10 cells' voltage; vbat8 is for 20 cells' voltage and vbat12 is for 30 cells' voltage. If NIMH_VPKOL (EEPROM register 26h, bit7) is 1, only the vbat12 time slot is present without the vbat4, vbat8 time slots; if NIMH_VPKOL is 0, vbat4, vbat8, vbat12 time slots are all present.

(4) The "µP req" indicates the ADC request from the Microprocessor which can be 13~16bits. In one ADC cycle, at least one Microprocessor ADC request can be completed. The Microprocessor will not launch new ADC request until the previous ADC request is finished. In OZ890, there is an ADC busy bit (bit0 in Operation Register 25h) to inform the Microprocessor that the ADC request is being processed; also OZ890 will provide ADC event bit (bit6 in Operation Register 2bh) to tell the Microprocessor that the ADC request is completed. The specified ADC request channel and its resolution are set in Operation Register 24h.

(5) If ET1, ET2 and ET3 external temperature are enabled, adc cycle1, adc cycle2, adc cycle3, adc cycle4 will be repeated; if only ET1 and ET2 external temperatures are enabled, adc cycle1, adc cycle2, adc cylce4 will be repeated; if only ET1 external temperature is enabled, adc cycle1, adc cylcle4 will be repeated; if there is no external temperature, only adc cycle4 will be repeated.

Battery Protection

OZ890 includes a digital Battery Protection Engine (BPE), which can operate independently from the Microprocessor. The BPE constantly monitors data from the ADC and other circuits described below. If a protection error condition is detected and persists for certain time, the BPE will force the charge and/or discharge MOSFET off. If some vital safety condition, such as extremely high cell voltage or extremely low cell voltage or un-balance cell voltage happens, or the Power MOSFET fails, or in Software Mode, OZ890 loses communication with host, the BPE will assert the Permanent Failure (PF) signal to instruct an optional external fuse circuit to permanently disable the battery pack. In Software Mode the chip provides an exclusive pin ALERTN to send the error message to Microprocessor besides forcing the charge and/or discharge MOSFET off when error condition happens. In Hardware mode, the BPE takes over the Protection and Release actions while in Software Mode, the chip only takes Protection actions and it fully relies on the Microprocessor's decision for release actions.

Over-current (OC)

OZ890 includes an independent hardware over-current detector that monitors the current that flows through the sense resistor to detect over-current condition in either charge or discharge. If the over-current condition continues for a programmable delay time, the protection circuit will turn off the charge and discharge MOSFETs. In sleep mode, OC detection is not available, only when sleep wakeup timer has expired or there is wakeup by I2C access, or SC event, the OZ890 will return to full power mode, and then OC detection is available. The charge and discharge over-current thresholds are set in EEPROM Registers 28h and 29h.

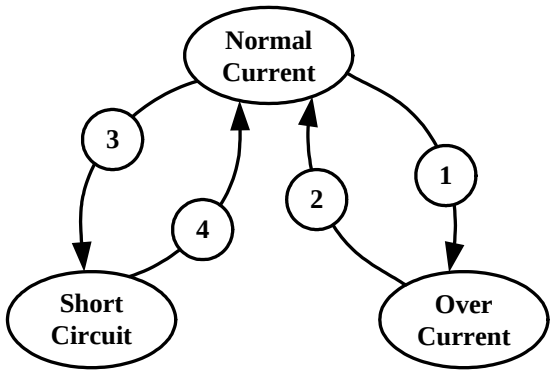


Fig.3 OC&SC State Machine

Charge Voc:10mV to 105mV, 5mV steps.
Discharge Voc: -285mV to -30mV, -5mV steps.

The real OC value is the Voc/Rs, where Rs is current sense resistor value. The over-current delay allows the system to momentarily accept a high current condition. The delay time can be programmed from 2ms to 16.3sec with OCDN4 – OCDN0 (bit[7:3] of EEPROM register 2ah) and OCDS2 – OCDS0 (bit[2:0] of EEPROM register 2ah). Charge and discharge OC share the same delay time. Charge OC release delay time and discharge OC release delay time can be programmed from 1s to 32s with COCRC2 – COCRC0 (bit[2:0] of EEPROM Register 2dh) and DOCRC2 – DOCRC0 (bit[5:3] of EEPROM Register 2dh) respectively. OZ890 also supports an external manual release function. After discharge OC happens, the chip will be released from discharge OC protection condition when the input analog signal of pin SCRL comes back to the normal level, this function is enabled by setting DOCRC2 – DOCRC0 to "000".

In OZ890, the offset canceling function is provided for charge over-current and discharge over-current detectors. The offset values are stored with COCO3 – COCO0 (bit[7:4] of EEPROM Registers 03h) and DOCO3 – DOCO0 (bit[7:4] of EEPROM Registers 04h) which are set at ATE test stage and cannot be modified after ATE_FRZ (bit7 of EEPROM Register 25h) is set to "1". The real charge and discharge OC thresholds are the values calibrated by the offsets. Please refer to the description of ***EEPROM Registers 28h and 29h*** in the section "Detailed EEPROM Registers Information" for details.

By employing the offset canceling function, OZ890 can ensure the OC protection accuracy. Please see the application note "***OZ890 AN-19: Resolution and Accuracy of OZ890 Cell Voltage and Temperature Measurement and accuracy of OC/SC Protection***" for details.

If users use the sense resistor to measure the current, set NO_SNSR (bit7 in EEPROM 27h) to be "0" and OC/SC protection works; if users use other method (Hall Device, for example) instead of sense resistor to measure current through GPIO[3], set NO_SNSR to be "1" and the OC/SC protection does not work .

Short-circuit (SC)

Short circuit detection is very similar to over-current detection. When short circuit condition is detected, OZ890 will turn off the charge and discharge MOSFETs. Short circuit threshold Vsc can be programmed from -620mV to -50mV in -10mV steps with SCC5 – SCC0 (bit[5:0] of EEPROM register 2bh). The real current is Vsc/Rs. Short circuit delay time can be programmed from 8us to 32.8ms with SCDN4 – SCDN0 (bit[7:3] of EEPROM register 2ch) and SCDS2 – SCDS0 (bit[2:0] of EEPROM register 2ch). SC release delay time is from 0.25min to 1.75min in 0.25min steps, which is configured by SCRC2 – SCRC0 (bit[7:5] of EEPROM register 30h). OZ890 also supports an external manual release function. After SC happens, the chip will be released from SC protection condition when the input analog signal of pin SCRL comes back to the normal level, this function is enabled by setting SCRC2 – SCRC0 to "000".

In OZ890, the offset canceling function is provided for short-circuit detector. The offset value is stored with SCO3 – SCO0 (bit[3:0] of EEPROM Registers 03h) which is got at ATE test stage and cannot be modified after ATE_FRZ (bit7 of EEPROM Register 25h) is set to "1". The real short-circuit threshold is the value calibrated by the offset. Please refer to the description of ***EEPROM Register 2bh*** in the section "Detailed EEPROM Registers Information" for details.

By employing the offset canceling function, OZ890 can ensure the SC protection accuracy. Please refer to the application note "***OZ890 AN-19: Resolution and Accuracy of OZ890 Cell Voltage and Temperature Measurement and accuracy of OC/SC Protection***" for details.

In real application, the battery pack often has high current transients. These transients can cause voltage spikes across the sense resistors that may accidentally trigger the SC protection of OZ890. So a low pass filter must be inserted into the current detection path and the PCB layout along this path must be treated carefully. Please refer to the application note "***OZ890 AN-15: PCB Layout Guideline***" for details.

Description of States (Fig. 3)

State	Description
Normal Current	No OC, SC event; Permit charge and discharge if no other protection events
Short Circuit	Prohibit discharge, charge and pre-charge if pre-charge function is enabled If SCRC2 – SCRC0 !='000', wait for the timer release If SCRC2 – SCRC0 ='000', wait for external short circuit condition being removed
Over Current	Prohibit discharge, charge and pre-charge if pre-charge function is enabled Waiting for the timer release for Charge OC If DOCRC2 – DOCRC0 !='000', wait for the timer release for discharge OC If DOCRC2 – DOCRC0 ='000', wait for external discharge OC condition being removed

Transition Description (Fig. 3)

Transition	Initial State	Condition		Final State
		Hardware Mode	Software Mode	
1	Normal Current	OC event occurs (charge (or discharge) current ⩾ charge (or discharge) OC threshold & delay timer expires)		Over Current
2	Over Current	In charge condition: release delay timer expires; In discharge condition: release delay timer expires or external release happens.	Microprocessor makes decision	Normal Current
3	Normal Current	SC event occurs (discharge current ⩾ SC threshold & delay timer expires)		Short Circuit
4	Short Circuit	Release timer expires or external release happens	Microprocessor makes decision	Normal Current

In sleep mode, OZ890 SC threshold and delay time setting in EEPROM are invalid. SC protection is based on the voltage of pin SCRL. When SCRL reaches about 1V, SC protection happens, and OZ890 will try to immediately turn off MOSFET. But different MOSFET and PCB layout may cause different SC threshold and delay time.

In sleep mode, SCRL detection also wakes up the OZ890 when SC happens.

Over-voltage (OV)

Figure 4 shows the cell voltage protection state machine. The protection engine performs over-voltage detection by comparing 13-bit values from the ADC with an OV threshold which is programmed in EEPROM Registers 4ah and 4bh. When over-voltage condition is detected, OZ890 will turn off the charge MOSFET after a delay time. This delay time can be programmed from 1 second to 16 seconds in 1 second step with OVUVD3 – OVUVD0 (bit[3:0] of EEPROM register 2eh). When cell voltage is less than the OV release value and persists for the specified time (same as the OV protection delay time), OZ890 Protection Engine will quit the OV condition and turn on the charge MOSFET. The OV release value also can be programmed in EEPROM registers 4ch and 4dh. The OV release value should set lower than OV threshold. In sleep mode, OV detection is not available, only when sleep wakeup timer has expired or there is wakeup by I2C access, or SC event, the OZ890 will return to full power mode, and then OV detection is available.

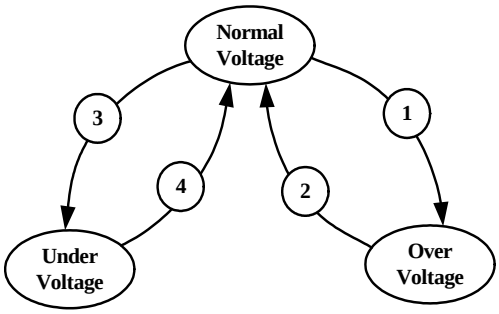


Fig. 4 OV/UV state machine

Under-voltage (UV)

Under-voltage protection operates in the same way as over-voltage protection. When under-voltage condition is detected, OZ890 will turn off discharge MOSFET after a specified delay time. In sleep mode, UV detection is not available, only when sleep wakeup timer expired or wakeup by I2C access, or SC event, the OZ890 will return to full power mode, and then UV detection is available. Its threshold can be programmed in EEPROM Registers 4eh and 4fh. UV release value can be programmed in EEPROM Registers 50h and 51h. The UV release value should be set higher than UV threshold. Under-voltage protection and release has the same delay time as the over-voltage protection and release.

States Description (Fig. 4)

State	Description
Normal Voltage	No OV, UV event; Permit charge, discharge if no other protection events
Over Voltage	Prohibit charge; Permit discharge if no other protection events; if discharge current exists, that is discharge current < discharge state threshold, turn on charge MOSFET
Under Voltage	Prohibit discharge; When pre-charge function is enabled, if Vcell < UV threshold, permit pre-charge but prohibit charge; if Vcell ⩾ UV threshold, permit pre-charge and charge if no other protection events; When pre-charge function is not enabled, prohibit pre-charge but permit charge if no other protection events; If charge current exists, that is charge current > charge state threshold, turn on discharge MOSFET

Transition Description (Fig. 4)

Transition	Initial State	Condition		Final State
		Hardware Mode	Software Mode	
1	Normal Voltage	• OV event occurs (Vcell ⩾ OV threshold & delay timer expires)		Over Voltage
2	Over Voltage	• OV event clears (Vcell < OV release value & delay timer expires)	Microprocessor makes decision	Normal Voltage
3	Normal Voltage	• UV event occurs (Vcell ⩽ UV threshold & delay timer expires);		Under Voltage
4	Under Voltage	• UV event clears (Vcell > UV release value & delay timer expires)	Microprocessor makes decision	Normal Voltage

Thermal Protection (OT and UT)

Thermal protection is performed based on inputs from both the internal temperature sensor and the optional external temperature sensors. Thermal information may be used to temporarily interrupt the charge cycle and/or disable discharge. OZ890 provides both under temperature (UT) and over temperature (OT) protection. In sleep mode, OT/UT detection is not available, only when sleep wakeup timer expired or wakeup by I2C access, or SC event, the OZ890 will return to full power mode, then OT/UT detection is available. Both OT and UT thresholds are programmable. External over temperature (OTE) threshold setting is in EEPROM Registers 56h and 57h, OTE release value programmed in EEPROM Registers 58h and 59h. External under temperature (UTE) threshold is set up in EEPROM Registers 5ah and 5bh, UTE release value programmed in EEPROM Registers 5ch and 5dh. Internal over temperature (OTI) threshold setting is in EEPROM Registers 5eh and 5fh. OTI release value is programmed in EEPROM Registers 60h and 61h. Internal under temperature (UTI) threshold setting is in EEPROM Registers 62h and 63h. UTI release value is programmed in EEPROM Registers 64h and 65h. External and Internal OT/UT protection and release delay time can be programmed from 1 TSP (Temperature Scan Period) to 16 TSP in 1 TSP steps with OTUTD3 – OTUT0 (EEPROM register 2eh, bit[7:4]).

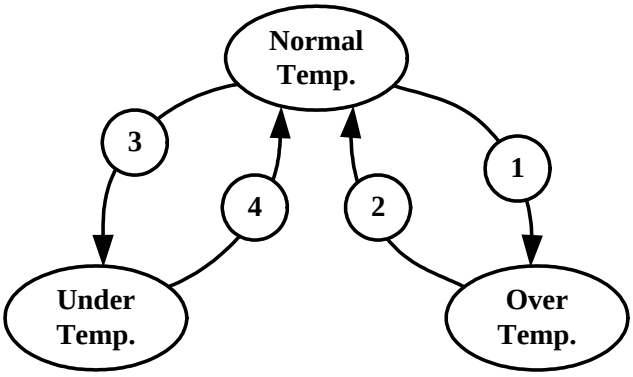


Fig.5 Temperature Protection State Machine

States Description (Fig. 5)

State	Description
Normal Temp	Internal UT threshold < Internal Temperature < Internal OT threshold; External UT threshold < External Temperature < External OT threshold; Permit charge and discharge if no other protection events
Over Temp.	Prohibit charge and discharge; Prohibit pre-charge if pre-charge function is enabled
Under Temp.	Prohibit charge; Prohibit pre-charge if pre-charge function is enabled; Permit discharge if no other protection events; If discharge current exists, that is discharge current < discharge state threshold, OZ890 will turn on charge MOSFET

Transition Description (Fig. 5)

Transition	Initial State	Condition		Final State
		Hardware Mode	**Software Mode**	
1	Normal Temp.	• OT event occurs (External (or Internal) temperature) ≥ External (or Internal) OT threshold & delay timer expires)		Over Temp.
2	Over Temp.	• OT event clears (External temperature < External OT release value & Internal temperature < Internal OT release value & delay timer expires)	Microprocessor makes decision	Normal Temp.
3	Normal Temp.	• UT event occurs (External (or Internal) temperature) ≤ External (or Internal) UT threshold & delay timer expires)		Under Temp
4	Under Temp	• UT event clears (External temperature > External UT release value & Internal temperature > Internal UT release value & delay timer expires)	Microprocessor makes decision	Normal Temp

Permanent Failure (PF) protection

Extremely high cell voltage PF (VHPF) & Extremely low cell voltage PF (VLPF)
There are two Permanent Failure voltage thresholds, one is extremely high cell voltage PF threshold which is programmed in EEPROM Registers 52h and 53h, and the other is extremely low cell voltage PF threshold which is programmed in EEPROM Registers 54h and 55h. If any cell voltage is lower than the latter or higher than the former for the specified time, OZ890 will assert a PF signal to blow the external fuse and the pack will be in permanent failure condition. This function acts as the secondary voltage protection and can be disabled by setting VHPF_ENB (EEPROM register 2fh, bit5) and VLPF_ENB (EEPROM register 2fh, bit4). The PF delay time can be programmed from 2s to 32s in 2s steps with PFD3 – PFD0 (EEPROM register 2fh, bit[3:0]).

There is no VHPF protection For NiMH battery application.

Extremely un-balanced cell voltage PF (CUPF)
When the cells get aged, the unbalance between cells may become worse. When a voltage mismatch between cells reaches a threshold value programmed in EEPROM register 46h and 47h, the cell unbalance is detected. In Hardware Mode, if the cell unbalance is detected for a period of time (same as the PF delay time), it will send out PF and go into Shut Down Mode. In Software Mode, once the cell unbalance is detected, it will make pin ALERTN active to inform the Microprocessor. The Microprocessor can read the corresponding event register and take the corresponding action. There is no dedicated CUPF enable/disable bit. In order to disable CUPF, EEPROM Registers 46h and 47h can be set to a very large value so that it cannot be triggered.

The CUPF function can be employed to implement the cell disconnection detection. Please refer to the application note "***OZ890 AN-14: Cell Disconnection Detection***" for details

Power MOSFET Failure PF (MFPF)
When the charge and Pre-charge MOSFET are both off and OZ890 still detects some current flowing into the battery pack and its value is larger than the charge state threshold, or when the discharge MOSFET is off and OZ890 detects some current flowing out of the battery pack and its value is less than the discharge state threshold, the MOSFET failure is detected. In Hardware Mode, if the MOSFET failure is detected for a period of time (same as the PF delay time), OZ890 will send out PF signal and goes into Shut Down Mode. In Software Mode, once the MOSFET failure is detected, it will make pin ALERTN active to inform the Microprocessor. The Microprocessor can read the corresponding event register and take the corresponding action. This function can be enabled by setting MFPF_ENB (bit6 of EEPROM register 2fh).

Deadman PF (DMPF)
Further, in OZ890 Software Mode, there is a deadman PF event. OZ890 provides a deadman function to check the communication between external Microprocessor and OZ890. In Hardware Mode, the deadman function is always disabled. In Software Mode, OZ890 will increment the deadman timer every second. If "DMN_C2 – DMN_C0" bits are all 0, the deadman check is disabled; if "DMN_C2 – DMN_C0" (bit[2:0] in Operation Register 1ah) are a non-zero value, the deadman check is enabled.

The deadman check function needs the periodic handshake protocol between the Microprocessor and OZ890. When a successful handshake happens, the deadman timer is cleared before it reaches the "Allowed Max Deadman Time". If the communication between Microprocessor and OZ890 is blocked or the Microprocessor hangs, the deadman timer expires and the deadman event occurs.

When the deadman check is enabled, the Microprocessor is required to do as follows within the specified time period:

- Check the deadman timer (bit[5:0] in Operation Register 1bh)
- Write "1" into CLR_TM (bit6 in Operation Register 1bh) to clear the deadman timer

If the handshake between Microprocessor and OZ890 is normal, the Microprocessor will clear the deadman timer before it expires so that no deadman event will occur. If the handshake has some problem, the Microprocessor cannot clear the deadman timer in time so that the deadman timer expires after the "Allowed Max Deadman Time" specified by DMN_C2 – DMN_C0. As a result, the deadman PF event will occur.

DMN_RST_ENB (bit3 in Operation Register 1ah) selects OZ890's action to the deadman event. If set to "1", OZ890 will send out a 64ms low active pulse to RSTN pin to reset the external Microprocessor; if set to "0", OZ890 will turn off all the MOSFETs and send out a PF signal and then shut down itself.

Power Mode

To save power, OZ890 works in different power mode according to the system status. In Hardware Mode, there are 4 power modes: Full Power Mode, Idle Mode, Sleep Mode and Shut Down Mode. In Software Mode, the Idle Mode concept does not apply.

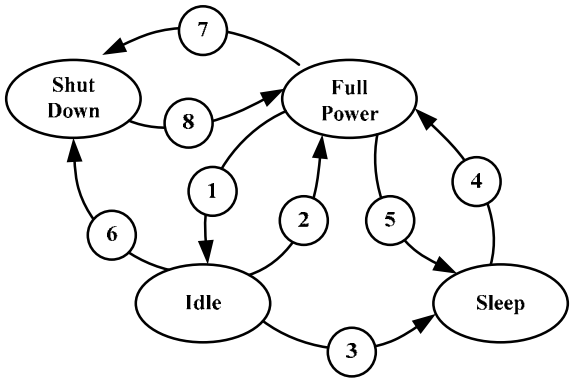


Fig. 6 OZ890 Power Mode Diagram

Mode Description (Fig.6)

Mode	Description
Full Power	Normal voltage, temp. and current scan (period: 1S) Safety protection check Power Consumption < 1.5mA (I_{VCC}) The ON/OFF state of the Charge, Pre-charge and Discharge MOSFET: refer to the "Power MOSFET Driver Control" section
Idle	Slower voltage, temp. and current scan period (configuration through bit6:4 in EEPROM register 27h : 1~56s step:8s) Safety protection check Power consumption < 150uA (I_{VCC}, during the period when ADC scan is stopped) The ON/OFF state of the Charge, Pre-charge and Discharge MOSFET: refer to the "Power MOSFET Driver Control" section
Sleep	Stop voltage, temp. and current scan Stop safety protection check except for SC protection based on SCRL pin Most blocks are powered down, only internal backup 3.3V and 2.5V(Software Mode) power supply and wakeup block enable Power consumption < 50uA (I_{VCC}) The ON/OFF state of the Charge, Pre-charge and Discharge MOSFET: refer to the "Power MOSFET Driver Control" section
Shut Down	All block disabled except backup 3.3V power supply, backup 2.5V power supply and I2C wakeup circuit Power consumption < 30uA (I_{VCC}) The ON/OFF state of the Charge, Pre-charge and Discharge MOSFET: all off.

Transition Description(Fig.6)

Transition	Initial Mode	Condition	Final

		Hardware Mode	Software Mode	Mode
1	Full Power	No charge/discharge and No OV, OT, UT, OC, SC event occurs, No bleeding event occurs (if bleeding enable bit is set), No PF(VHPF, VLPF, CUPF, MFPF) event occurs for 5 minutes ***Note:*** *OZ890 can enter idle mode in UV event.*	No Idle Mode concept in Software Mode.	Idle
2	Idle	Charge/discharge or Any OV, OT, UT, OC, SC event occurs, Any PF(VHPF, VLPF CUPF, MFPF) event occurs or Bleeding event occurs	No Idle Mode concept in Software Mode.	Full Power
3	Idle	No charge/discharge and No OV, OT, UT, OC, SC event occurs, No bleeding event occurs (if bleeding enable bit is set), No PF(VHPF, VLPF, CUPF, MFPF fail) event occurs for 10 minutes ***AND*** Sleep mode support bit (bit5 of EEPROM 33h) is "1" ***Note:*** *OZ890 can enter sleep mode in UV event.*	No Idle Mode concept in Software Mode.	Sleep
4	Sleep	I2C bus active ***OR*** Sleep timer expires ***OR*** External SC event happens ***Note:*** *Because OZ890 needs some time when it first wakes up from Sleep Mode, if it is waken up by I2C access, it will send out "nak" to respond to the first I2C access, so the first I2C access is likely to fail. Host software needs to re-send the I2C command after getting the "nak".*		Full Power
5	Full Power	➢ If no event occurs after wakeup directly from the sleep mode ***AND*** ➢ sleep mode support bit (bit5 of EEPROM 33h) is "1"	Microprocessor makes decision. Please refer to the application note "***OZ890 AN-12: Sleep Mode Implementation in Software Mode***" for details.	Sleep
6	Idle	EFETC shut down ***OR*** Host write shutdown	No Idle Mode concept in Software Mode.	Shut Down
7	Full Power	EFETC shut down ***OR*** PF event shut down ***OR*** Host write shutdown ***OR*** Deadman shutdown in Software Mode		Shut Down
8	Shut Down	➢ EFETC goes low wake up (only for EFETC shut down) ***OR*** ➢ RSTN reset wake up ***OR*** ➢ I2C activity wake up		Full Power

Internal/External Bleeding

To keep the balance among battery cells, OZ890 can do cell bleeding for Li-ion batteries when the cells are charged or idle in Hardware Mode. OZ890 will not do cell bleeding for NiMH batteries in any conditions. OZ890 supports internal bleeding and external bleeding. For internal bleeding, the current will be 10mA~15mA for the thermal consideration, and only supports the highest cell bleeding; for the external bleeding, bleeding current is decided by external bleeding resistor Rb (Fig. 7), and can support 1, 2, 3, 4 or all cell bleeding simultaneously.

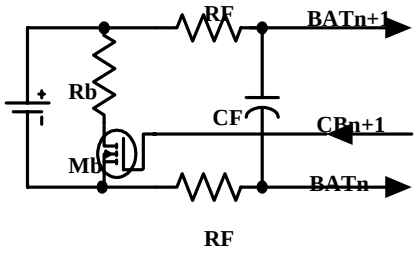


Fig.7 External Bleeding Diagram

We can enable the bleeding with BS (bit3 in EEPROM register 33h), select external/internal bleeding with SEB (bit2 in EEPROM register 33h) and set the maximum external bleeding cell number with BCNC1 – BCNC0 (bit[1:0] in EEPROM register 33h) or set BLD_ALL_EN (bit2 in EEPROM register 32h) to bleed up to 12 cells if they meet the bleeding condition.

BSV12 – BSV0 (EEPROM register 48h, 49h) specifies the bleeding start voltage and BA2 – BA0 (bit[2:0] in EEPROM register 48h) specifies the bleeding accuracy.

OZ890 has embedded O2micro "Balance on Demand (BOD)" technology which starts up bleeding when the following conditions are all satisfied:

- Battery pack is in charge state (current larger than the charge state threshold) or in idle state (current smaller than the charge state threshold and larger than the discharge state threshold) if idle bleeding is enabled by setting bit6 in EEPROM register 2dh.
- The bleeding function is enabled
- The highest cell voltage exceeds the bleeding start voltage
- The cell voltages' difference exceeds the bleeding accuracy
- No error event, like OT, UT, OV, UV, OC, SC. If any error event happens, bleeding stops right away.

In Software Mode, OZ890 cannot do cell balancing automatically. But it can balance the cells at any time with accessing Operation Register 22h, 23h by Microprocessor. Once cell bleeding has been turned on by Microprocessor, it remains active until the Microprocessor turns it off. When an error condition (OV, UV, OC, SC, OT, UT) occurs, the cell bleeding will be paused; when the error disappears, the cell bleeding will be resumed. Please refer to the Application Note "***OZ890 AN-13: Cell Balance Implementation in Software Mode***".

Pre-Charge

OZ890 provides the Pre-charging function. When the configurable parameter PS (bit4 in EEPROM Register 33h) is "1", the pre-charge function is enabled; when it is "0", the pre-charge function is disabled.

When the pre-charge function is enabled, during the time from UV detection to UV release,

(a) If the lowest voltage of the cells is less than the UV threshold (13-bit UVT12 – UV0 in EEPROM Register 4eh, 4fh), the pre-charge MOSFET will be turned ON and charge MOSFET will be turned OFF.
(b) If the lowest voltage of the cells is greater than the UV threshold, but less than the UV release value (13-bit UVR12 – UVR0 in EEPROM Register 4ch, 4dh), the pre-charge MOSFET is still ON and charge MOSFET will be turned ON if no other protection event occurs.

If the lowest voltage of the cells is greater than the UV release value, the pre-charge MOSFET will keep in its previous state and charge MOSFET is still ON if no other protection event occurs. Note that if some events like OC or OV happen before the lowest voltage of the cells rise to the UV release value, the pre-charge MOSFET will be off and keep in off state after all cells' voltage return to normal range.

When the pre-charge function is disabled, the pre-charge MOSFET will be turned off always.

Internal Temperature Sensor

OZ890 takes advantage of silicon device physics and circuit design technology for the internal temperature sensor. The internal temperature sensor generates a voltage level which is proportional to the temperature. As shown in Fig. 8, with a temperature increase of 1°C, internal temperature sensor output voltage will increase by 2.0976mV. The internal temperature range is -40°C~120°C.

External Temperature Sensor

OZ890 provides 3 GPIO ports for external temperature detection; the application circuitry is shown in Fig. 9. In Hardware Mode, GPIO1 and GPIO2 can be configured as external temperature measurement channels by enabling the T1E and T2E bits in EEPROM register 32h. In Software Mode, GPIO1, GPIO2 and GPIO3 can be configured as external temperature measurement channels by setting Operation Register 2dh. We recommend a 103 NTC type thermistor.

The R(t) characteristics of 103 NTC Thermistor is shown in Fig. 10. The sensed voltage V(t) characteristics is shown Fig. 11. For example, according to the circuit in Fig.9, Vt2=3.3V * RT2 / (RB2 + RT2). Please refer to the Application Note "***OZ890 AN-4: Using External Thermistor***" for details of how to use External Thermistor to measure temperature. Note that the driver voltage at GPIO0 is only effective during external temperature detection.

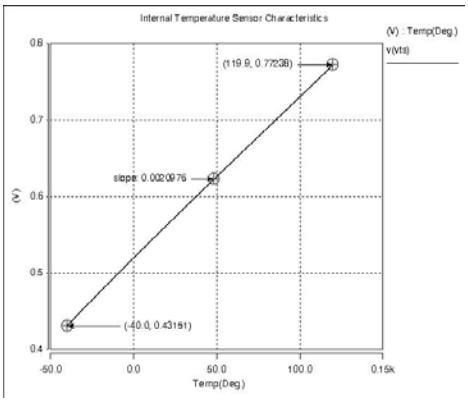


Fig.8 Internal Temperature Sensor Curve

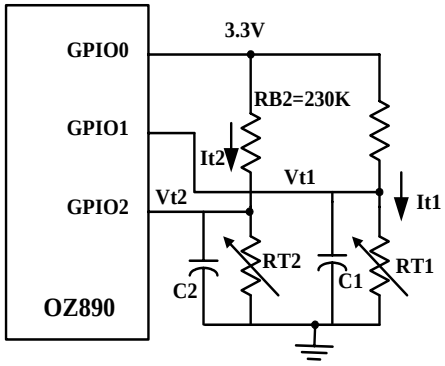


Fig.9 External Temperature Sensor Application

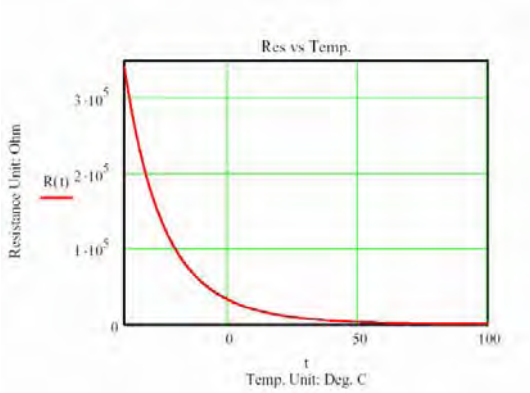


Fig.10 Thermistor RT characteristics

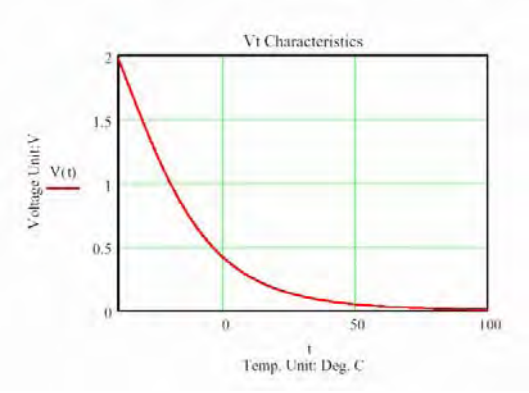


Fig.11 The sensed voltage Vt characteristics

Power MOSFET Driver Control

Patent pending smart MOSFET driver supports charge, pre-charge and PWM discharge. When working with Microprocessor, the discharge current can be controlled by pulse width of the discharge MOSFET control signal. The driver also supports parallel and series charge/discharge loop.

In Hardware Mode, the charge/discharge MOSFET is fully controlled by Battery Protection Engine (BPE) state machine. Refer to the “Battery Protection” section for detailed information.

In Software Mode, Battery Protection Engine in OZ890 forces the pre-charge, charge or discharge MOSFETs off when error condition happens. However the release actions are left to be decided by the Microprocessor. The pre-charge, charge and discharge MOSFETs can be respectively controlled through PCHG_ENB, CHG_ENB and DSG_ENB (Operation Register 1eh, bit[2:0]).

The PWM discharge frequency is configured by PWM_FC1 – PWM_FC0 (Operation Register 1dh, bit[5:4]. The frequency range is 1kHz ~ 8kHz and the pulse duty is 0 ~ 100%, which is controlled by PWM_DC3 – PWM_DC0 (Operation Register 1dh, bit[3:0]). These register bits can be configured by the Microprocessor when working in the Software Mode.

OZ890 also provides a pin (EFETC) for external MOSFET control signal input or internal MOSFET control signal output; it makes the MOSFET control very flexible.

The discharge MOSFET gate-to-source voltage (the voltage at pin DSG) is clamped to 11V (typical) when MOSFET is in ON state; the CHG and PCHG pins have internally embedded a 5uA sink current for P-type charge and pre-charge MOSFET driver or level shift for N-type charge and pre-charge MOSFET driver. MOSFET driver circuits are shown in Fig.12 and Fig.13.

The Application Note "***OZ890 AN-3***" describes how to drive the external MOSFETs; the Application Note "***OZ890 AN-9***" describes how to use EFETC pin to implement the PWM control of the discharge MOSFET in Hardware Mode as well as Software Mode; **t**he Application Note "***OZ890 AN-10***" describes how to use the EFETC pin as power switch and MOSFET switch.

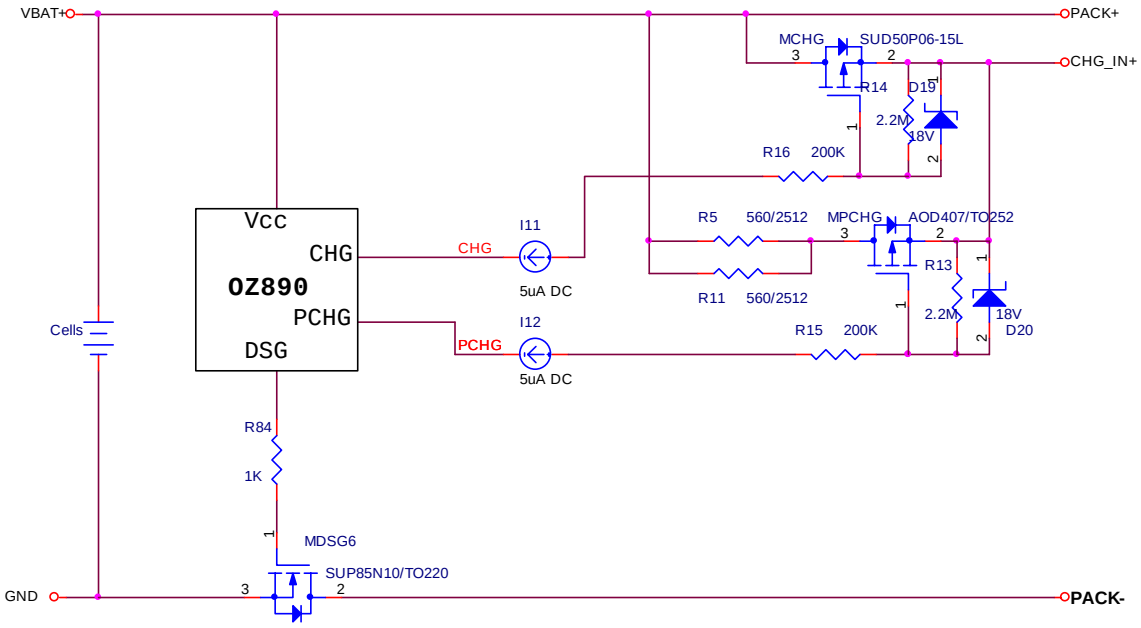


Fig.12 MOSFET drive circuit with P-type charge and pre-charge MOSFET

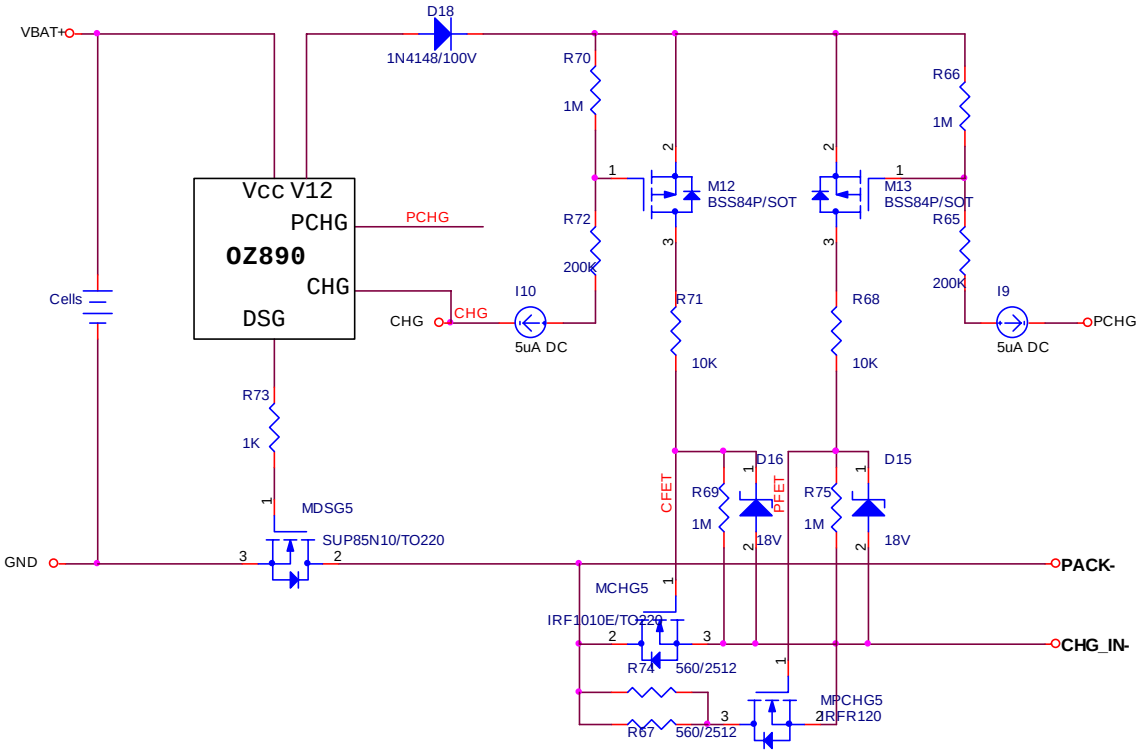


Fig.13 MOSFET drive circuit with N-type charge and pre-charge MOSFET

Voltage Based Gas Gauge (V-GG)

In Hardware Mode, OZ890 has voltage based gas gauge function. The method is to look up the battery capacity table according to the lowest voltage of the cells for the Li-ion battery or the V_{BAT8} for the 20S NiMH battery or the V_{BAT12} for the 30S NiMH battery. In the embedded EEPROM, there are 10 bytes (66h~6fh) which are used to specify the 5 voltage references so that OZ890 can display the 5 levels of battery capacity by LED0~LED4. When LED4/GPIO2 is configured as external temperature channel, only LED0~LED3 can be used to display 4 levels of battery capacity; and there are 8 bytes (66h~6dh) being used to specify the 4 voltage references.

In Software Mode, this voltage based gas gauge function is disabled. The Microprocessor can do coulomb counting based gas gauge.

There are 5×13 Bits of EEPROM space for lookup table data set in registers 66h-6fh, that correspond to five variables: GaugeV1 –GaugeV5.

Working Mode	**Hardware Mode**			**Software Mode**		
Battery Type	M. Li-ion	P. Li-ion	NiMH(20S/30S)	M. Li-ion	P. Li-ion	NiMH(20S/30S)
Lookup Table	GaugeV1: 13Bits EEPROM (20% or 25%)			Coulomb Counting Based Gas Gauge		
	GaugeV2: 13Bits EEPROM (40% or 50%)					
	GaugeV3: 13Bits EEPROM (60% or 75%)					
	GaugeV4: 13Bits EEPROM (80% or 100%)					
	GaugeV5: 13Bits EEPROM (100%)					

LED Error Display

OZ890 can display the 5-level or 4-level battery capacity based on voltage gas gauge function via LED0~LED4 or LED0~LED3. Additionally OZ890 also can display the safety events controlled by NO_ER_DSPL (bit7 of EEPROM Register 2dh). If NO_ER_DSPL is set to “0”, the LED Error Display function is enabled; if NO_ER_DSPL is set to “1”, the LED Error Display function is disabled.

If the LED Error Display function is enabled, when OV, UV, OT, UT, OC, SC events happen or authentication fails, the normal gas gauge display will be disabled; instead the OV, UV, OT, UT, OC, SC events or authentication failure will be displayed as follows:

Errors	**LED Function**
OC or SC event	LED0 blinks in 1Hz (0.5s display on; 0.5s display off).
OV event	LED1 blinks in 1Hz (0.5s display on; 0.5s display off).
OT event	LED2 blinks in 1Hz (0.5s display on; 0.5s display off).
UT event	LED3 blinks in 1Hz (0.5s display on; 0.5s display off).
Authentication failure	LED2, LED3 blinks in 1Hz (0.5s display on; 0.5s display off).
No safety event	Normal 5-level or 4-level battery capacity display

If the LED Error Display function is disabled (NO_ER_DSPL is set to “1”) even if OV, UV, OT, UT, OC, SC events or authentication failure happen, the normal gas gauge will be displayed normally on the LEDs.

Authentication Function

For better safety, OZ890 provides the authentication mechanism for the charging operation and/or the discharging operation. The authentication is processed between OZ890 and the charger/load. If the authentication fails, OZ890 will turn off the charge/discharge MOSFET so that OZ890 cannot work with the unauthorized charger/load.

The authentication function can be disabled, or only enabled for charge operation or only for discharge operation, or for both, which is configured by ATHCC1 – ATHCC0 (bit[1:0] in EEPROM register 7fh). To guarantee the security, OZ890 will check authentication data 2 times in one authentication cycle.

The basic authentication flow is as follows:

(1) Charger/load reads out the 16-bit authentication random number ATH_NM15 – ATH_NM0 (Operation Register 6bh and 6ch);

(2) Charger/load calculates the 16-bit authentication data with 16-bit random number ATH_NM15 – ATH_NM0 using the authentication algorithm, which is the same as OZ890's internal algorithm specified by the 16-bit authentication code ATHC15 – ATHC0 (EEPROM register 7ch and 7dh);

(3) Charger/load writes back the 16-bit calculated authentication data ATH_D15 – ATH_D0 (Operation Register 6dh and 6eh).

(4) OZ890 calculates the 16-bit authentication data internally using the same random number and compare with ATH_D15 – ATH_D0 in Operation Register 6dh and 6eh.

(5) If the authentication data is matched, then repeats step 1 to 4 another time. If the second authentication data also matches, then authentication passes; if any authentication data does not match, the authentication fails. The authentication status can be read-out in ATH_DSG_FAIL, ATH_DSG_OK, ATH_CHG_FAIL and ATH_CHG_OK (Bit3 – Bit0 in Operation Register 6fh).

(6) For charge authentication, it starts at the beginning of the charging operation and the charger should finish the step (1) to step (5) within 30 seconds. Otherwise, OZ890 will consider this as failed charge authentication and turn off the charge MOSFET to stop charge.

For discharge authentication, it starts at the beginning of the discharging operation and the load should finish the step (1) to step (5) within 30 seconds. Otherwise, OZ890 will consider this as failed discharge authentication and turn off the discharge MOSFET to stop discharge.

External Clock Selection

After power on reset, OZ890 selects the internal clock as working clock by default. To get the more accuracy data or keep the synchronization with the external Microprocessor, the external TCLK clock can be selected as working clock. When the RSTN pin is low, if the external clock TCLK has 16 clocks, TCLK will be switched as working clock. Once TCLK is used as working clock, it will be remained until the next Power On Reset. Note when the RSTN pin is high, even the external clock TCLK has toggles, TCLK will not be switched as working clock. The external clock frequency can be 4MHz, 2MHz, 1MHz or 512KHz specified by TCLK_F1 – TCLK_F0 (bit[7:6] in Operation Register 23h).

Serial Communication Bus

With the serial communication bus, the external Microprocessor or host can access directly Operation Register 00h ~ 7fh and access indirectly EEPROM Register 00h~7fh via Operation Register 5ch ~ 5fh. OZ890 supports 3 kinds of serial bus protocol to communicate. In all cases, OZ890 chip acts as slave device.

BSEL1, BSEL0 (Pin30, Pin31)	Bus Type Description
2'b00	2-wire I2C bus
2'b01	4-wire I2C bus (unilateral bus)
2'b10	O2Micro defined PBus serial bus protocol.
2'b11	Reserved.

2-wire I2C Bus

In this case, Pin 26 is input clock pin and the clock comes from external I2C host, Pin 28 is the bi-directional data pin. For detailed I2C protocol and timing information, please refer to the I2C Specifications.

4-wire I2C Bus

In this case, Pin 25 is the output clock pin (SCLO) and Pin 26 is the input clock pin (SCL), Pin 27 is the output data pin (SDAO), Pin 28 is the input data pin (SDA). This bus protocol and timing is the same as 2-wire I2C bus except separating input/output line.

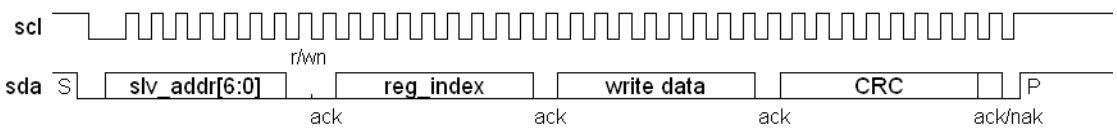
4-wire I2C bus is easy to work with external general purpose Microprocessor and opto-coupler, it will be useful in some non-common ground and/or noisy application. It only can be used in Software Mode. Please refer to the Application Note ***"OZ890 AN-2"*** for the usage of the OZ890 4-wire I2C communication interface.

I2C PEC

To get the higher reliability in the I2C communication, OZ890 has a PEC (Packet Error Check) option. If the configurable parameter PEC_ENB (bit4 in EEPROM Register 30h) is set to "1", the PEC check is enabled; if set to "0", the PEC is disabled. At default, the PEC_ENB bit is "0" to disable the PEC check.

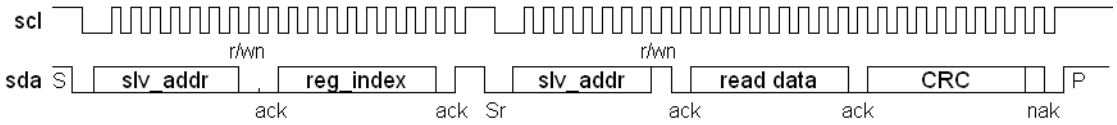
OZ890 supports one-byte I2C write with PEC, one-byte I2C read with PEC. All bytes after I2C START are used to do PEC check. The CRC generation polynomial= x^8+x^2+x+1 is used to do PEC check.

The timing for one-byte I2C write with PEC is shown below:



If the PEC check is ok, the write data will be written into the register, and the “ack” is returned to the I2C master. If the CRC check is in error, the write data is regarded as corrupted so that it cannot be written into the registers, then “nak” is returned to tell the I2C master there is an error in the cycle.

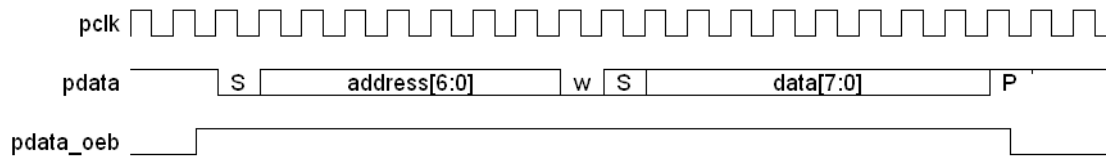
The timing for one-byte I2C read with PEC is shown below:



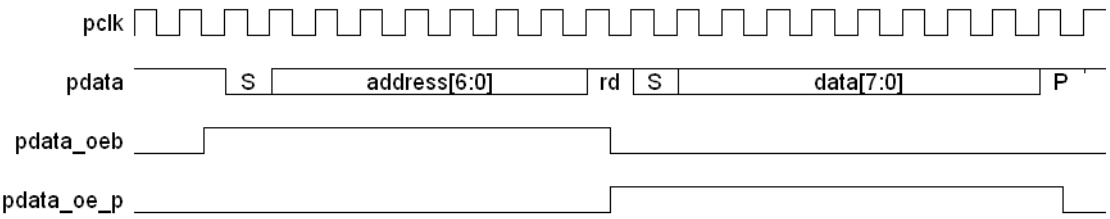
If the CRC check is ok, the read data will be regarded as correct data by the I2C master; if the CRC check is in error, the read data will be regarded as corrupted. No matter whether the CRC check is ok or not, the I2C master will send out “nak” to tell OZ890 to terminate this I2C read. If the CRC check is in error, the I2C master will re-read the data or take other actions after this cycle.

PBus

PBus is O2Micro defined low-cost serial bus. It will work with O2Micro’s Microprocessor solution. There are 2 signals in the PBus: one is clock signal PCLK; the other is bidirectional data signal PDATA. The PCLK (Pin 26) of PBus is output from OZ890, so the synchronization between PBus clock and the internal clock will be relatively simple.



The above timing diagram is a write operation to a register in OZ890 from Microprocessor. The signal called pdata_oe_b is the output enable on PDATA pin on the Microprocessor side. “S” means start bit; “P” means stop bit. The serial bus will be high when idle. Reads and writes both begin with a “start” bit followed by 7 address bits, allowing 128 registers to be accessed. After the last address bit, the rd/wr# bit indicates the transfer direction (low for write, as shown above). After the rd/wr# bit is a second start bit, followed by 8 data bits. After the final data bit, a stop bit finishes the transfer. The transmitting device switches PDATA on the rising edge of PCLK. The receiving device can strobe the results on the falling edge of PCLK.



The above timing diagram is a read operation from a register in OZ890. The address byte is sent by the Microprocessor as before. In the middle of the rd/wr# bit, the Microprocessor tri-states its PDATA driver and OZ890 turns on its PDATA driver. The signal called pdata_oe_p is the output enable on PDATA pin in OZ890 side.

After the rd/wr# bit, the second start bit and data byte are driven by OZ890. The timing for read operation is identical to the timing for write operation. The “start” bit at the start of the data byte is a way to verify that OZ890 is responding to the read request. After the data byte has been transferred, OZ890 will disable its PDATA driver in the middle of the stop bit.

The Microprocessor can start another read or write transfer immediately after the stop bit. Each read or write takes 19 cycles of PCLK.

Bus Disconnection

I2C/PBus actually is board level communication bus and not recommended to do hot plugging. Because hot plugging surge current and other noise may cause wrong data to be written into certain registers, especially during I2C/PBus is under accessing.
Please refer to ***OZ890 Application Alert–1:Direction for I2C Bus Disconnection*** for details.

EEPROM AND OPERATION REGISTERS MAP

OZ890 has 128-byte built-in EEPROM Registers (00h-7fh) and 128-byte Operation Registers (00h-7fh). EEPROM Registers are used to store important battery pack, battery cell information and configure the OZ890 chip. Operation Registers are used to store ADC instant data, OZ890 status information, and to control OZ890 state-machine, etc. When system is powered on, the data in EEPROM Registers 26h-33h, 7ch-7fh will be loaded into the Operation Registers 06h-13h, 7ch-7fh respectively. Fig. 14 shows the configuration of EEPROM Registers and Operation Registers.

Serial Bus (I2C or PBus) can directly access Operation Registers. It can also indirectly access EEPROM Registers through Operation Registers 5ch ~ 5fh.

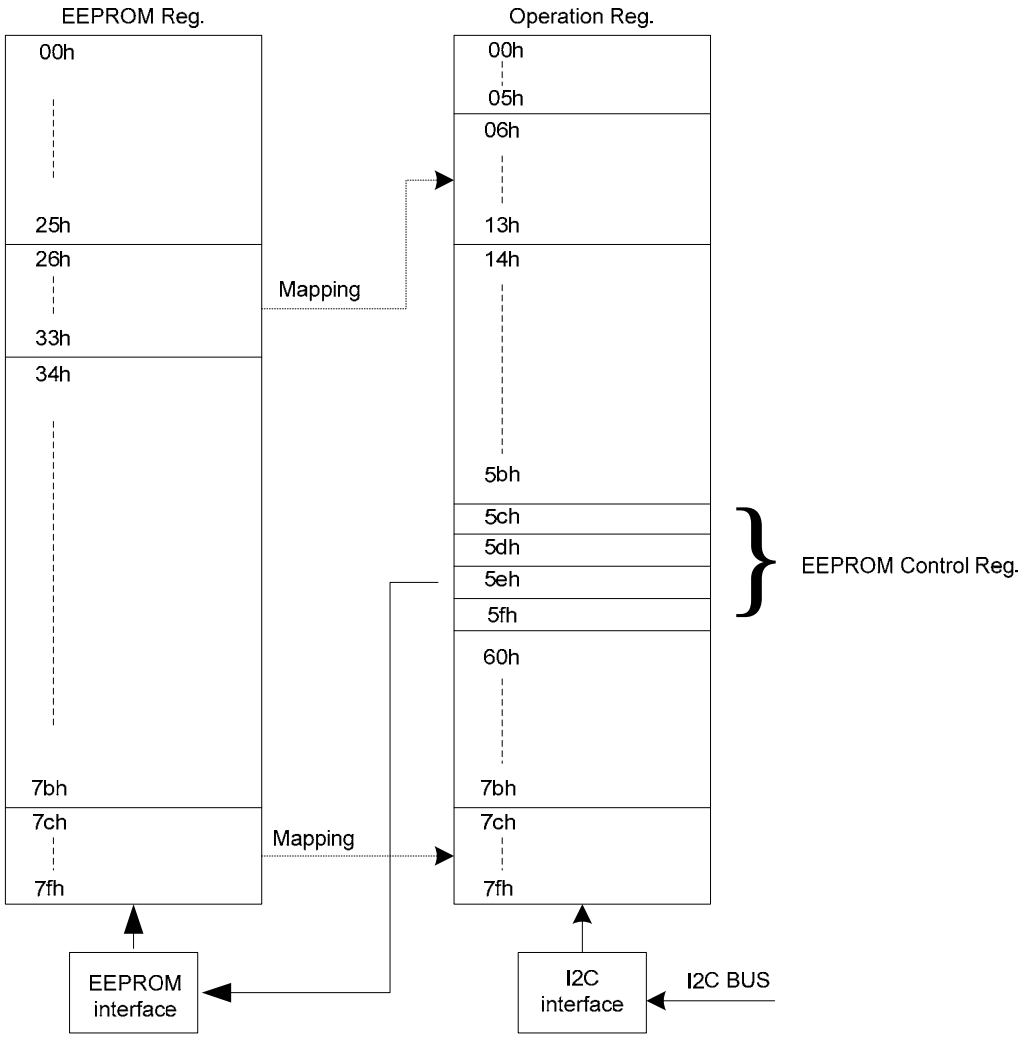


Fig. 14 Configuration of EEPROM Register and Operation Register

EEPROM Registers

EEPROM Access

EEPROM Registers are used to store important battery pack and battery cell information, protection parameters and OZ890 chip configuration, etc. The writing, reading and mapping of EEPROM Registers to Operation Registers can be executed by accessing Operation Register 5ch~5fh. Please refer to the descriptions of ***Operation Register 5ch ~ 5fh*** in the section "Detailed Operation Registers Information" and the application note "***OZ890 AN-6: Software Mode Guide***" for details.

EEPROM Registers are divided into 3 sections. In order to prevent that important information from accidentally being erased or illegally accessed, each section has individual "freeze" bits to control the access limitation.

EEPROM Section	Description
00h~25h ATE data	This section is reserved for internal trimming data which is decided at ATE test stage. ATE_FRZ (Bit 7 in EEPROM register 25h) controls the access to ATE data. ATE_FRZ =0: all can be read and written. ATE_FRZ =1: 00h~11h, 16h~17h and 1eh~25h can be read but cannot be written; 12h~15h and 18h~1dh can be read and written.
26h~6fh User data	This section is used for programmable parameters for battery protection and management. 26h~33h are mapped into the Operation Registers 06h~13h; 34h~6fh are not mapped into the Operation Registers. UC1 – UC0 (Bit7 – Bit6 in EEPROM register 33h) control the access to User data (Note UC1 – UC0 bits can be read out always). UC1 – UC0 = "00": the safety scan is disabled; 26h~6fh can be read and written. UC1 – UC0 = "01": the safety scan is enabled; 26h~6fh can be read and written. UC1 – UC0 = "10": the safety scan is enabled; 26h~6fh is read only. UC1 – UC0 = "11": the safety scan is enabled; 26h~33h and 46h~6fh cannot be read and written; 34h~45h is read only.
70h~7fh Secret data	This section stores the secret information, such as password, authentication code, etc. 70h~7bh are not mapped into the Operation Registers. 7ch~7fh are mapped into the Operation Registers 7ch~7fh. STFRZ (Bit7 in EEPROM register 7fh) controls the access to Secret data (Note STFRZ bit can be read out always). STFRZ = "0": secret data section can be read and written. STFRZ = "1": secret data can't be accessed at all.

Before the OZ890 chip is delivered to customers, the ATE_FRZ bit is always programmed to "1", the UC1 – UC0 bits are always programmed to "01" and STFRZ bit is always programmed to "0". After the user data and secret data is programmed, customers can set "UC1 – UC0 " to "11" or "10", or set "STFRZ" to "1" so that user data and secret data cannot be directly modified any more. However, if customers are not satisfied with the previous data, the EEPROM Protected Data Modification Mechanism can be employed to update the EEPROM data.

EEPROM Protected Data Modification Mechanism

In the EEPROM Protected Data Modification Mechanism, the internal trimming data in EEPROM will be read-out at first, then erased, then written back. If the writing back is not executed successfully, the internal trimming data in EEPROM will be lost. So the mechanism should be executed very carefully. Following gives the detailed flow:

(1) Read out the current EEPROM data and save them.
- (a) Read out the ATE data (ATE data is always readable) and save in the buffer.
- (b) Read out the user data and save in the buffer (If the user data is not readable, this step can be skipped).
- (c) Read out the secret data and save in the buffer (If the secret data is not readable, this step can be skipped).

(2) Pass password verification.
- (a) Set OZ890 into EEPROM mode by setting EE_MD2 – EE_MD0 (Bit6 – Bit4 in Operation Register 5fh) to ”101”. This operation will enable the EEPROM access and stop the safety scan.
- (b) Enter PWD15 – PWD0 (Operation Register 69h/6ah). OZ890 allows entering password up to 8 times. In the 8 times, if the password is matched with the one stored in the EEPROM register 69h/6ah, the password verification is ok (PWD_OK = 1); if no matched password is found, the password verification will fail (PWD_FAIL = 1). Once the password verification has failed, the password failure will be kept and no password can be verified until power on reset. Note that the external reset pin will not clear the password failure.
- (c) Check password verification status in PWD_FAIL, PWD_OK, PWD_BUSY (Bit7 – Bit5 in Operation Register 6fh) until PWD_BUSY is “0”.
  If PWD_OK is “0” and PWD_FAIL is “0”, go to step (b) of (2);

  If PWD_OK is “1”, the password verification is ok, exit EEPROM mode by clearing EE_MD2 – EE_MD0 to “000”, go to step (3);

  If PWD_OK is “0” and PWD_FAIL is “1”, the password verification has failed, exit EEPROM mode by clearing EE_MD2 – EE_MD0 to “000”, the EEPROM modification is aborted and exited.

(3) Do EEPROM block-erase to erase all EEPROM data.

(4) Do EEPROM mapping to unfreeze the EEPROM write.

(5) Modify the data in buffer and write back to EEPROM
- (a) Modify the user data or secret data in buffer.
- (b) Write back the ATE data into EEPROM.
- (c) Write back the user data into EEPROM.
- (d) Write back the secret data into EEPROM.

(6) Do EEPROM mapping.

EEPROM Registers Map

Reg index (hex)	EEPROM Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
00-01	ATE Data	reserved for internal trimming data							
02	Internal Temperature Offset	INTO7	INTO6	INTO5	INTO4	INTO3	INTO2	INTO1	INTO0
03	COC, SC Offset	COCO3	COCO2	COCO1	COCO0	SCO3	SCO2	SCO1	SCO0
04	DOC Offset	DOCO3	DOCO2	DOCO1	DOCO0	reserved	reserved	reserved	reserved
05	Cell1 Voltage 2nd Offset	CV1SO7	CV1SO6	CV1SO5	CV1SO4	CV1SO3	CV1SO2	CV1SO1	CV1SO0
06	Cell2 Voltage 2nd Offset	CV2SO7	CV2SO6	CV2SO5	CV2SO4	CV2SO3	CV2SO2	CV2SO1	CV2SO0
07	Cell3 Voltage 2nd Offset	CV3SO7	CV3SO6	CV3SO5	CV3SO4	CV3SO3	CV3SO2	CV3SO1	CV3SO0
08	Cell4 Voltage 2nd Offset	CV4SO7	CV4SO6	CV4SO5	CV4SO4	CV4SO3	CV4SO2	CV4SO1	CV4SO0
09	Cell5 Voltage 2nd Offset t	CV5SO7	CV5SO6	CV5SO5	CV5SO4	CV5SO3	CV5SO2	CV5SO1	CV5SO0
0a	Cell6 Voltage 2nd Offset	CV6SO7	CV6SO6	CV6SO5	CV6SO4	CV6SO3	CV6SO2	CV6SO1	CV6SO0
0b	Cell7 Voltage 2nd Offset	CV7SO7	CV7SO6	CV7SO5	CV7SO4	CV7SO3	CV7SO2	CV7SO1	CV7SO0
0c	Cell8 Voltage 2nd Offset	CV8SO7	CV8SO6	CV8SO5	CV8SO4	CV8SO3	CV8SO2	CV8SO1	CV8SO0
0d	Cell9 Voltage 2nd Offset	CV9SO7	CV9SO6	CV9SO5	CV9SO4	CV9SO3	CV9SO2	CV9SO1	CV9SO0
0e	Cell10 Voltage 2nd Offset	CV10SO7	CV10SO6	CV10SO5	CV10SO4	CV10SO3	CV10SO2	CV10SO1	CV10SO0
0f	Cell11 Voltage 2nd Offset	CV11SO7	CV11SO6	CV11SO5	CV11SO4	CV11SO3	CV11SO2	CV11SO1	CV11SO0
10	Cell12 Voltage 2nd Offset	CV12SO7	CV12SO6	CV12SO5	CV12SO4	CV12SO3	CV12SO2	CV12SO1	CV12SO0
11	Cell13 Voltage 2nd Offset	CV13SO7	CV13SO6	CV13SO5	CV13SO4	CV13SO3	CV13SO2	CV13SO1	CV13SO0
12	GPIO1 2nd Offset	G1SO7	G1SO6	G1SO5	G1SO4	G1SO3	G1SO2	G1SO1	G1SO0
13	GPIO2 2nd Offset	G2SO7	G2SO6	G2SO5	G2SO4	G2SO3	G2SO2	G2SO1	G2SO0
14	GPIO3 2nd Offset	G3SO7	G3SO6	G3SO5	G3SO4	G3SO3	G3SO2	G3SO1	G3SO0
15	Reserved	reserved							
16	Current 2nd Offset	CSO7	CSO6	CSO5	CSO4	CSO3	CSO2	CSO1	CSO0
17		CSO15	CSO14	CSO13	CSO12	CSO11	CSO10	CS09	CSO8
18	PF Record	reserved	reserved	reserved	CUPF	MFPF	VHPF	VLPF	DMPF
19-1d	Reserved	reserved							
1e-24	ATE Data	reserved for internal trimming data							

Reg index (hex)	EEPROM Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
25	ATE Freeze	ATE_FRZ	reserved	reserved	reserved	reserved	reserved	reserved	reserved
26	Cell Number	NIMH_ VPKOL	reserved	BTYP1	BTYP0	CNUM3	CNUM2	CNUM1	CNUM0
27	Scan Rate	NO_SNSR	SCN_RT2	SCN_RT1	SCN_RT0	reserved	EFETC_ SHDN_ ENB	EFETC1	EFETC0
28	Discharge state threshold and Charge OC Control	DCTC2	DCTC1	DCTC0	OCCFC4	OCCFC3	OCCFC2	OCCFC1	OCCFC0
29	Charge state threshold and Discharge OC Control	CCTC1	CCTC0	OCCFD5	OCCFD4	OCCFD3	OCCFD2	OCCFD1	OCCFD0
2a	OC Delay	OCDN4	OCDN3	OCDN2	OCDN1	OCDN0	OCDS2	OCDS1	OCDS0
2b	SC Control	reserved	reserved	SCC5	SCC4	SCC3	SCC2	SCC1	SCC0
2c	SC Delay	SCDN4	SCDN3	SCDN2	SCDN1	SCDN0	SCDS2	SCDS1	SCDS0
2d	OC Release Control	NO_ER_ DSPL	IDL_BLD_ ENB	DOCRC2	DOCRC1	DOCRC0	COCRC2	COCRC1	COCRC0
2e	OT/UT, OV/UV Delay Control	OTUTD3	OTUTD2	OTUTD1	OTUTD0	OVUVD3	OVUVD2	OVUVD1	OVUVD0
2f	PF Control	reserved	MFPF_ENB	VHPF_ENB	VLPF_ENB	PFD3	PFD2	PFD1	PFD0
30	I2C Address Config and SC Release Control	SCRC2	SCRC1	SCRC0	PEC_ENB	I2CADDR3	I2CADDR2	I2CADDR1	I2CADDR0
31	Wake Up Control	reserved	reserved	reserved	reserved	SLP_T3	SLP_T2	SLP_T1	SLP_T0
32	Mode Control	T2E	T1E	RSTN_ BYPASS	reserved	V_OFF_ DIS	I_OFF_ DIS	BLD_ ALL_EN	HM
33	Hardware Bleeding	UC1	UC0	SS	PS	BS	SEB	BCNC1	BCNC0
34	Sense Resistor	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
35	Reserved	reserved							
36~3f	Factory Name	FN7	FN6	FN5	FN4	FN3	FN2	FN1	FN0
40~44	Project Name	PN7	PN6	PN5	PN4	PN3	PN2	PN1	PN0
45	Version Number	VNR7	VNR6	VNR5	VNR4	VNR3	VNR2	VNR1	VNR0
46	Cell Unbalance Threshold	CUT4	CUT3	CUT2	CUT1	CUT0	reserved	reserved	reserved
47		CUT12	CUT11	CUT10	CUT9	CUT8	CUT7	CUT6	CUT5
48	Bleeding Start Voltage	BSV4	BSV3	BSV2	BSV1	BSV0	BA2	BA1	BA0
49		BSV12	BSV11	BSV10	BSV9	BSV8	BSV7	BSV6	BSV5
4a	OV Threshold	OVT4	OVT3	OVT2	OVT1	OVT0	reserved	reserved	reserved
4b		OVT12	OVT11	OVT10	OVT9	OVT8	OVT7	OVT6	OVT5
4c	OV Release	OVR4	OVR3	OVR2	OVR1	OVR0	reserved	reserved	reserved
4d		OVR12	OVR11	OVR10	OVR9	OVR8	OVR7	OVR6	OVR5
4e	UV Threshold	UVT4	UVT3	UVT2	UVT1	UVT0	reserved	reserved	reserved
4f		UVT12	UVT11	UVT10	UVT9	UVT8	UVT7	UVT6	UVT5
50	UV Release	UVR4	UVR3	UVR2	UVR1	UVR0	reserved	reserved	reserved
51		UVR12	UVR11	UVR10	UVR9	UVR8	UVR7	UVR6	UVR5
52	Extremely High Voltage Threshold	PFVH4	PFVH3	PFVH2	PFVH1	PFVH0	reserved	reserved	reserved
53		PFVH12	PFVH11	PFVH10	PFVH9	PFVH8	PFVH7	PFVH6	PFVH5

Reg index (hex)	EEPROM Reg Name	Bit Number							
		7	6	5	4	3	2	1	0
54	Extremely Low Voltage Threshold	PFVL4	PFVL3	PFVL2	PFVL1	PFVL0	reserved	reserved	reserved
55		PFVL12	PFVL11	PFVL10	PFVL9	PFVL8	PFVL7	PFVL6	PFVL5
56	OTE Threshold	OTET4	OTET3	OTET2	OTET1	OTET0	reserved	reserved	reserved
57		OTET12	OTET11	OTET10	OTET9	OTET8	OTET7	OTET6	OTET5
58	OTE Release	OTER4	OTER3	OTER2	OTER1	OTER0	reserved	reserved	reserved
59		OTER12	OTER11	OTER10	OTER9	OTER8	OTER7	OTER6	OTER5
5a	UTE Threshold	UTET4	UTET3	UTET2	UTET1	UTET0	reserved	reserved	reserved
5b		UTET12	UTET11	UTET10	UTET9	UTET8	UTET7	UTET6	UTET5
5c	UTE Release	UTER4	UTER3	UTER2	UTER1	UTER0	reserved	reserved	reserved
5d		UTER12	UTER11	UTER10	UTER9	UTER8	UTER7	UTER6	UTER5
5e	OTI Threshold	OTIT4	OTIT3	OTIT2	OTIT1	OTIT0	reserved	reserved	reserved
5f		OTIT12	OTIT11	OTIT10	OTIT9	OTIT8	OTIT7	OTIT6	OTIT5
60	OTI Release	OTIR4	OTIR3	OTIR2	OTIR1	OTIR0	reserved	reserved	reserved
61		OTIR12	OTIR11	OTIR10	OTIR9	OTIR8	OTIR7	OTIR6	OTIR5
62	UTI Threshold	UTIT4	UTIT3	UTIT2	UTIT1	UTIT0	reserved	reserved	reserved
63		UTIT12	UTIT11	UTIT10	UTIT9	UTIT8	UTIT7	UTIT6	UTIT5
64	UTI Release	UTIR4	UTIR3	UTIR2	UTIR1	UTIR0	reserved	reserved	reserved
65		UTIR12	UTIR11	UTIR10	UTIR9	UTIR8	UTIR7	UTIR6	UTIR5
66	Gas Gauge V1	GGVA4	GGVA3	GGVA2	GGVA1	GGVA0	reserved	reserved	reserved
67		GGVA12	GGVA11	GGVA10	GGVA9	GGVA8	GGVA7	GGVA6	GGVA5
68	Gas Gauge V2	GGVB4	GGVB3	GGVB2	GGVB1	GGVB0	reserved	reserved	reserved
69		GGVB12	GGVB11	GGVB10	GGVB9	GGVB8	GGVB7	GGVB6	GGVB5
6a	Gas Gauge V3	GGVC4	GGVC3	GGVC2	GGVC1	GGVC0	reserved	reserved	reserved
6b		GGVC12	GGVC11	GGVC10	GGVC9	GGVC8	GGVC7	GGVC6	GGVC5
6c	Gas Gauge V4	GGVD4	GGVD3	GGVD2	GGVD1	GGVD0	reserved	reserved	reserved
6d		GGVD12	GGVD11	GGVD10	GGVD9	GGVD8	GGVD7	GGVD6	GGVD5
6e	Gas Gauge V5	GGVE4	GGVE3	GGVE2	GGVE1	GGVE0	reserved	reserved	reserved
6f		GGVE12	GGVE11	GGVE10	GGVE9	GGVE8	GGVE7	GGVE6	GGVE5
70~79	reserved	reserved							
7a	Password	PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0
7b		PWD15	PWD14	PWD13	PWD12	PWD11	PWD10	PWD9	PWD8
7c	Authentication Code	ATHC7	ATHC6	ATHC5	ATHC4	ATHC3	ATHC2	ATHC1	ATHC0
7d		ATHC15	ATHC14	ATHC13	ATHC12	ATHC11	ATHC10	ATHC9	ATHC8
7e	Reserved	reserved							
7f	Authentication Control	STFRZ	reserved	reserved	reserved	reserved	reserved	ATHCC1	ATHCC0

Detailed Information about EEPROM Registers

EEPROM Register 02h – Internal Temperature Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INTO7	INTO6	INTO5	INTO4	INTO3	INTO2	INTO1	INTO0

This register is used to specify the internal temperature offset (2's complement code). Before the bit "ATE_FRZ" is set to "1", this register can be written or erased. After the bit "ATE_FRZ" is set to "1", this register cannot be written or erased, only can be read out.

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EEPROM Register 03h – COC, SC Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
COCO3	COCO2	COCO1	COCO0	SCO3	SCO2	SCO1	SCO0

This register is used to store the offsets for COC (Charge Over Current) and SCO (Short Circuit). Before the bit "ATE_FRZ" is set to "1", this register can be written or erased. After the bit "ATE_FRZ" is set to "1", this register cannot be written or erased, only can be read out.

Bit7 – Bit4 (COCO3 – COCO0): Specify COC's offset as N*5mv/Rs (Here Rs is the sense resistor value). N is 4-bit signed value and limited in the range of -6 ~ +6. The offset is measured in ATE test and used in setting COC threshold.

Bit3 – Bit0 (SCO3 – SCO0): Specify SC's offset as N*(-10mv)/Rs. N is 4-bit signed value and limited in the range of -3 ~ +3. The offset is measured in ATE test and used in setting SC threshold.

==========

EEPROM Register 04h – DOC Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOCO3	DOCO2	DOCO1	DOCO0	Reserved	reserved	reserved	reserved

This register is used to store the offsets for DOC (Discharge Over Current). Before the bit "ATE_FRZ" is set to "1", this register can be written or erased. After the bit "ATE_FRZ" is set to "1", this register cannot be written or erased, only can be read out.

Bit7 – Bit4 (DOCO3 – DOCO0): Specify DOC's offset as N*(-5mv)/Rs. N is 4-bit signed value and limited in the range of -6 ~ +6. The offset is measured in ATE test and used in setting DOC threshold.

==========

EEPROM Register 05h ~ 11h – Cell Voltage 2nd Offset Registers

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CVX[2]SO7	CVXSO6	CVXSO5	CVXSO4	CVXSO3	CVXSO2	CVXSO1	CVXSO0

These registers are used to do cell voltage ADC channels' 2nd offset cancellation. All values are 8-bit signed value with 1.22mv LSB. Before the bit "ATE_FRZ" is set to "1", these registers can be written or erased. After the bit "ATE_FRZ" is set to "1", these registers cannot be written or erased, only can be read out.

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EEPROM Register 12h ~ 14h – GPIO 2nd Offset Registers

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GX[3]SO7	GXSO6	GXSO5	GXSO4	GXSO3	GXSO2	GXSO1	GXSO0

These registers are used to do GPIO ADC channels' 2nd offset cancellation. All values are 8-bit signed value with 0.61mv LSB. These registers can be written or erased, no matter the bit "ATE_FRZ" is set to "1" or "0".

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[2] X is the number in 1~13.
[3] X is the number in 1~3.

EEPROM Register 16h/17h – Current 2nd Offset Registers

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CSO7	CSO6	CSO5	CSO4	CSO3	CSO2	CSO1	CSO0
CSO15	CSO14	CSO13	CSO12	CSO11	CSO10	CS09	CSO8

These registers are used to do current ADC channel's 2nd offset cancellation. The value is 16-bit signed value with 7.63uV/Rs LSB (Here Rs is the sense resistor value). Before the bit "ATE_FRZ" is set to "1", this register can be written or erased. After the bit "ATE_FRZ" is set to "1", this register cannot be written or erased, only can be read out.

==========

EEPROM Register 18h – PF Record Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	reserved	CUPF	MFPF	VHPF	VLPF	DMPF

This register saves the PF event record.

Bit4 (CUPF): Cell voltage unbalance PF record.

Bit3 (MFPF): MOSFET failure PF record.

Bit2 (VHPF): Cell voltage over extremely high voltage threshold PF record.

Bit1 (VLPF): Cell voltage under extremely low voltage threshold PF record.

Bit0 (DMPF): Deadman timer expired PF record.

When any individual PF event happens, the related PF record bit will be set to "1". Even if the ATE_FRZ bit in EEPROM register 25h is set, this register is still writeable.

==========

EEPROM Register 25h – ATE Freeze Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ATE_FRZ	reserved	reserved	reserved	reserved	reserved	reserved	reserved

This register freezes EEPROM ATE section.

Bit7 (ATE_FRZ): When set to "1", freeze ATE data section. EEPROM Registers 00h~11h, 16h~17h and 1eh~25h can be read but cannot be written; EEPROM Registers 12h~15h and 18h~1dh can be read and written.

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EEPROM Register 26h – Cell Number Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NIMH_VPKOL	reserved	BTYP1	BTYP0	CNUM3	CNUM2	CNUM1	CNUM0

This register selects the cell number, battery type and controls the checking for NiMH battery.

Bit3 – Bit0 (CNUM3– CNUM0): These 4 bits specify the number of Li-ion cells in series in the battery pack:

CNUM3– CNUM0	Cell Count	CNUM3– CNUM0	Cell Count
0101	5	1010	10
0110	6	1011	11
0111	7	1100	12
1000	8	1101	13
1001	9	Others	Reserved

Bit5 - Bit4 (BTYP1–BTYP0): These 2 bits indicate battery type

BTYP1– BTYP0	Battery type
00	30S NiMH
01	20S NiMH
10	Phosphate Li-ion
11	Cobalt/Manganese Li-ion

Bit7: This bit is used to control the voltage checking for NiMH battery. For 20S NiMH battery, if this bit is "1", only vbat8 will be checked; if this bit is "0", vbat4, vbat8 will be checked. For 30S NiMH battery, if this bit is "1", only vbat12 will be checked; if this bit is "0", vbat4, vbat8, vbat12 will be checked.

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EEPROM Register 27h – Scan Rate Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NO_ SNSR	SCN_RT2	SCN_RT1	SCN_RT0	reserved	EFETC_ SHDN_ENB	EFETC1	EFETC0

This register specifies the scan period and configuration of the EFETC pin function.

Bit1 – Bit0 (EFETC1– EFETC0): These 2 bits are used to define the EFETC pin's function when EFETC_SHDN_ENB register bit is "0", as shown in the following table:

EFETC1– EFETC0	EFETC Pin function
00	Input pin to control charge MOSFET. If "1", disable charge MOSFET; if "0", the charge MOSFET is controlled by the internal logic.
01	Input pin to control discharge MOSFET. If "1", disable discharge MOSFET; if "0", the discharge MOSFET is controlled by the internal logic.
10	Input pin to control charge/discharge MOSFET. If "1", disable charge MOSFET and discharge MOSFET; if EFETC is "0", the charge MOSFET and discharge MOSFET are controlled by the internal logic.
11	Output pin. It will output the discharge MOSFET control logic (If the discharge MOSFET is turned on, output "HIGH"; if the discharge MOSFET is turned off, output "LOW").

When EFETC_SHDN_ENB register bit is "1", EFETC1 & EFETC0 are ignored.

Bit2 (EFETC_SHDN_ENB): Enable EFETC pin as external shut down signal. If "1", enable EFETC pin as shut down control input pin (when EFETC is "1", shut down OZ890; when EFETC is "0", the system will work normally.); if "0", EFETC pin function controlled by the EFETC1 & EFETC0 bits.

Bit6 – Bit4 (SCN_RT2 – SCN_RT0): In Hardware Mode, these 3 bits are used to specify the scan period in Idle Mode; in Software Mode, these 3 bits are also used to specify the scan period, but the software can change the scan rate anytime by setting bit[6:4] of Operation Register 07h. The following table shows the details:

SCN_RT2 – SCN_RT0	Scan period
000	1s
001	8s
010	16s
011	24s
100	32s
101	40s
110	48s
111	56s

Bit7 (NO_SNSR): If set to “1”, it means no sense resistor is used. The current ADC channel is disabled and the ADC time slot for it will be used by GPIO3 channel if Operation Register 2dh, bit[7:6]=”11”; If set to “0”, it means the sense resistor is used.

==========

EEPROM Register 28h – Discharge state threshold and Charge OC Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DCTC2	DCTC1	DCTC0	OCCFC4	OCCFC3	OCCFC2	OCCFC1	OCCFC0

Bit7 – Bit5 (DCT2 – DCT0): Specify the current threshold for discharge state as shown below:

DCTC2 - DCTC0	Discharge state threshold
3’b000	-12*CRRT_LSB/Rs
3’b001	-24*CRRT_LSB/Rs
3’b010	-48*CRRT_ LSB/Rs
3’b011	-72*CRRT_LSB/Rs
3’b100	-108*CRRT_LSB/Rs
3’b101	-144*CRRT_LSB /Rs
3’b110	-192*CRRT_LSB /Rs
3’b111	-250*CRRT_LSB /Rs

***Note**: When the sensed voltage at the current sensor resistor is within the range from -10mV to 10mV, the Discharge State Threshold of the OZ890TN could have ±0.5mV error while that of the OZ890HTN could have ±0.3mV error.*

When NO_SNSR (Bit 7 in EEPROM Register 27h) is set to “0” (the current sensor resistor is used), CRRT_LSB (LSB of current channel) is 7.63uV; Rs is the sense resistor value. When NO_SNSR (Bit 7 in EEPROM Register 27h) is set to “1” (the current sensor resistor is not used) and G3_MD1 – G3_MD0 (Bit[7:6] in Operation Register 2dh) is set to “11” (the GPIO3 is used to detect the current from such as the hall device), the CRRT_LSB is the LSB of the GPIO3 channel specified by G3_RES1 – G3_RES0(Bit[5:4] in Operation Register 2dh) and Rs is the ratio between the hall voltage and the current. Refer to “GPIO3 ADC Data Register” for details of the LSB of the GPIO3 channel.

If the current < Discharge State Threshold, the chip will be regarded in discharge state; otherwise the chip is not in discharge state.

Bit4 – Bit0 (OCCFC4 – OCCFC0): Configure the COC (charge over current) threshold as (N+M-4)*5mv/Rs. Here, N is 5-bit unsigned value OCCFC4-OCCFC0 and M is 4-bit signed value COCO3-COCO0. (M is measured in ATE test and stored in EEPROM register 0x03, M is limited in the range -6~+6). **COC threshold is limited in (10mv~105mv)/Rs with 5mv/Rs step.**

Giving a COC threshold TH and M, we have the following formula:

$$TH = (N+M-4)*5/Rs$$

By solving the above formula, we can get N as

$$N = TH*Rs/5 - M + 4$$

Using the condition $10mv \le TH*Rs \le 105mv$, we can get N’s range as follows:

$$6 – M \le N \le 25 - M$$

==========

EEPROM Register 29h – Charge state threshold and Discharge OC Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CCTC1	CCTC0	OCCFD5	OCCFD4	OCCFD3	OCCFD2	OCCFD1	OCCFD0

Bit7 - Bit6 (CCTC1-CCTC0): Specify the current threshold for charge state as follows:

CCTC1-CCTC0	Charge state threshold
2’b00	12*CRRT_LSB/Rs
2’b01	24*CRRT_LSB/Rs
2’b10	48*CRRT_LSB/Rs
2’b11	120*CRRT_LSB/Rs

***Note**: When the sensed voltage at the current sensor resistor is within the range from -10mV to 10mV, the Charge State Threshold of the OZ890TN could have ±0.5mV error while that of the OZ890HTN could have ±0.3mV error.*

When NO_SNSR (Bit 7 in EEPROM Register 27h) is set to "0" (the current sensor resistor is used), CRRT_LSB (LSB of current channel) is 7.63uV; Rs is the sense resistor value. When NO_SNSR (Bit 7 in EEPROM Register 27h) is set to "1" (the current sensor resistor is not used) and G3_MD1 – G3_MD0 (Bit[7:6] in Operation Register 2dh) is set to "11" (the GPIO3 is used to detect the current from such as the hall device), the CRRT_LSB is the LSB of the GPIO3 channel specified by G3_RES1 – G3_RES0 (Bit[5:4] in Operation Register 2dh) and Rs is the ratio between the hall voltage and the current. Refer to "GPIO3 ADC Data Register" for details of the LSB of the GPIO3 channel.

If the current > Charge State Threshold, the chip will be considered to be in charge state; otherwise it is not in charge state.

Bit5 - bit0 (OCCFD5 - OCCFD0): Configure the DOC (discharge over current) threshold as (N+M)*(-5mv)/Rs. Here, N is 6-bit unsigned value OCCFD5-OCCFD0 and M is 4-bit signed number DOCO3-DOCO0. (M is measured in ATE test and stored in EEPROM 04h, M is limited in -6~+6). **DOC threshold is limited in (-285m ~ -30mv)/Rs with (-5mv)/Rs step.**

Giving a DOC threshold TH and M, we have the following formula:

$$TH = (N+M)*(-5)/Rs$$

By solving the above formula, we can get N as

$$N = TH*Rs/(-5) - M$$

Using the condition -285mv ≤ TH*Rs ≤ -30mv, we can get N's range as shown below:

$$6 - M \le N \le 57 - M$$

==========

EEPROM Register 2ah – OC Delay Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCDN4	OCDN3	OCDN2	OCDN1	OCDN0	OCDS2	OCDS1	OCDS0

This register sets over current delay time (for both DOC and COC).

Bit2 – Bit0 (OCDS2 – OCDS0): Define the OC delay unit as follows:

OCDS2 – OCDS0	OC delay unit
000	2ms
001	6ms
010	14ms
011	30ms
100	62ms
101	126ms
110	254ms
111	510ms

Bit7 – Bit3 (OCDN4 – OCDN0): Define the over current delay number as N+1 (N is the 5 bits unsigned value).
The OC delay time= (N+1) × (OC delay unit), so its range is 2ms~16.3s.
==========

EEPROM Register 2bh – SC Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	SCC5	SCC4	SCC3	SCC2	SCC1	SCC0

Bit5 - bit0 (SCC5 – SCC0): Configure SC (short circuit) threshold as (N+M+2)*(-10mv)/Rs.

Here, N is 6-bit unsigned value SCC5 – SCC0 and M is 4-bit signed number SCO3 – SCC0. (M is measured in ATE test and stored in EEPROM 03h, M is limited in -3~+3). **SC threshold is limited in (-620mv ~ -50mv)/Rs with (-10mv)/Rs step.**

Giving a SC threshold TH and M, we have the following formula:

$$TH = (N+M+2)*(-10)/Rs$$

By solving the above formula, we can get N as

$$N = TH*Rs/(-10) – M - 2$$

Using the condition -620mv ≤ TH*Rs ≤ -50mv, we can get N's range as shown below:

$$3 - M \le N \le 60 - M$$

Note: *The minimal value for the SC threshold is -620mV by design, but the minimal voltage for each of the SRN and SRP pins is -0.5V. Therefore, it is highly recommended that the setup for SC threshold does not fall below -500mV.*

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EEPROM Register 2ch – SC Delay Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCDN4	SCDN3	SCDN2	SCDN1	SCDN0	SCDS2	SCDS1	SCDS0

This register sets SC (short circuit) delay time.

Bit2 – Bit0 (SCDS2 – SCDS0): Define the short circuit delay unit.

SCDS2 – SCDS0	SC delay unit
000	8us
001	16us
010	32us
011	64us
100	128us
101	256us
110	512us
111	1024us

Bit7 – Bit3 (SCDN4 – SCDN0): Define the short circuit delay number as N+1 (N is the 5 bits unsigned value). The SC delay time= (N+1) × (SC delay unit), so its range is 8us~32.8ms.

==========

EEPROM Register 2dh – OC Release Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NO_ER_DSPL	IDL_BLD_ENB	DOCRC2	DOCRC1	DOCRC0	COCRC2	COCRC1	COCRC0

This register sets OC release delay time and release method.

Bit2 – Bit0 (COCRC2 – COCRC0): Configure the Charge OC release delay time.

COCRC2 – COCRC0	COC release delay time
3'b000	1s
3'b001	1s
3'b010	2s
3'b011	4s
3'b100	8s
3'b101	16s
3'b110	24s

3'b111	32s

Bit5 – Bit3 (DOCRC2 – DOCRC0): Configure the discharge OC release delay time.

DOCRC2 – DOCRC0	DOC release delay time
3'b000	External release. The DOC will be released by SCRL pin.
3'b001	1s
3'b010	2s
3'b011	4s
3'b100	8s
3'b101	16s
3'b110	24s
3'b111	32s

Bit6 (IDL_BLD_ENB): Enable idle bleeding in Hardware Mode. If set to "1", the battery can be bled in charge or idle mode; if set to "0", the battery can only be bled in charge state. In Software Mode, this bit is ignored.

Bit7 (NO_ER_DSPL): Disable the error display in Hardware Mode. In Software Mode, this bit is ignored. If set to "1", the errors such as OV, UV, OT, UT, OC, SC and authentication failure will not be displayed, the battery's capacity is always displayed. If set to "0", and the error(s) occurs, the error(s) will be displayed; if no error occurs, the battery's capacity is displayed.
==========

EEPROM Register 2eh – OT/UT, OV/UV Delay Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTUTD3	OTUTD2	OTUTD1	OTUTD0	OVUVD3	OVUVD2	OVUVD1	OVUVD0

This register sets OT/UT, OV/UV delay time.
Bit3 – Bit0 (OVUVD3 – OVUVD0): Configure the OV/UV delay time as (N+1) × (scan cycles).

Bit7 – Bit4 (OT/UT D3 – OT/UT D0): Configure the OT/UT delay time as (N+1) × (Temperature Scan Period, TSP).
==========

EEPROM Register 2fh – PF Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	MFPF_ENB	VHPF_ENB	VLPF_ENB	PFD3	PFD2	PFD1	PFD0

This register sets PF delay time and PF function enable/disable.

Bit3 – Bit0 (PFD3 – PFD0): Configure the VHPF/VLPF delay time as (2N+2) × (scan cycles). So, the PF delay is 2 ~ 32 scan cycles.

Bit4 (VLPF_ENB): Enable VLPF function if set to "1".

Bit5 (VHPF_ENB): Enable VHPF function if set to "1".

Bit6 (MFPF_ENB): Enable MOSFET failure detection function if set to "1". When this bit is "1", if the charge MOSFET and the pre-charge MOSFET are both turned off, but the chip is in charge state (current > the charge state threshold), the MOSFET will be regarded as having failed; on the other hand, if the discharge MOSFET is turned off, but the chip is in discharge state (current < the discharge state threshold), the MOSFET will be regarded as having failed. In Hardware Mode, if the MOSFET failure is detected for continuous time specified by the PF delay time, it will send out PF signal and shut down the system. In Software Mode, once the MOSFET failure is detected, it will make the pin ALERTN active to inform the Microprocessor, the Microprocessor can read the corresponding event register and take appropriate action.
==========

EEPROM Register 30h – I2C Address Configure and SC Release Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCRC2	SCRC1	SCRC0	PEC_ENB	I2CADDR3	I2CADDR2	I2CADDR1	I2CADDR0

This register sets up the OZ890 I2C address and SC release delay time and release method.

Bit3 – Bit0 (I2CADDR3 – I2CADDR0): Configure the I2C address as 60h + 2*N (N: 0~15).

Bit4 (PEC_ENB): Enable PEC (packet error check) in I2C protocol if set to "1". Refer to "I2C PEC" for detail.

Bit7 – Bit5 (SCRC2 – SCRC0): Configure the short-circuit release delay time.

SCRC2 – SCRC0	**SC release delay time**
3'b000	External release. The SC will be released by SCRL pin.
3'b001	0.25min (15 sec.)
3'b010	0.50min (30 sec.)
3'b011	0.75min (45 sec.)
3'b100	1.00min (60 sec.)
3'b101	1.25min (75 sec.)
SCRC2 – SCRC0	**SC release delay time**
3'b110	1.50min (90 sec.)
3'b111	1.75min (105 sec.)

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EEPROM Register 31h – Wake Up Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
31h	reserved	reserved	reserved	reserved	SLP_T3	SLP_T2	SLP_T1	SLP_T0

This register sets up the sleep timer when OZ890 enter sleep mode.

Bit3 – Bit0 (SLP_T3 – SLP_T0): The sleep timer control, which sets up the time interval to wakeup when OZ890 in sleep mode.

SLP_T3 – SLP_T0	**Sleep Time**
0000	Disable sleep timer wakeup function
0001	1 minute
N	N minute
1111	15 minute

==========

EEPROM Register 32h – Mode Control Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
32h	T2E	T1E	RSTN_ BYPASS	reserved	V_OFF_ DIS	I_OFF_ DIS	BLD_ ALL_EN	HM

This register selects the working mode and enables the external temperature sensors.
Bit0 (HM): Select Hardware Mode or Software Mode. If set to "1", select Hardware Mode; if set to "0", select Software Mode. In Hardware Mode, all controls are handled by OZ890 chip; in Software Mode, many controls such as bleeding are handled by the external Microprocessor.

Bit1 (BLD_ALL_EN): Enable bleeding all cells in Hardware Mode. If set to "1", all those cells meet the bleeding condition can be bled at the same time in Hardware Mode, not limited by the numbers defined in EEPROM register 33h, bit1-0; If set to "0", only 1~4 cells (defined by EEPROM register 33h, bit1-0) can be bled at the same time if they meet the bleeding condition. In Software Mode, this bit is ignored.

Bit2 (I_OFF_DIS): Disable the current 1st offset cancellation. If set to "1", the current 1st offset cancellation is disabled; if set to "0", the current 1st offset will be automatically cancelled.

Bit3 (V_OFF_DIS): Disable the voltage 1st offset cancellation. If set to "1", the voltage 1st offset cancellation is disabled; if set to "0", the voltage 1st offset will be automatically cancelled.

Bit5 (RSTN_BYPASS): This bit is used to control the rstn low pulse check function. If set to "1", OZ890 will start the ADC safety scan after power up regardless of the RSTN negative pulse; if set to "0", OZ890 will start the ADC safety scan after power up only after the negative pulse on the RSTN pin (pin 29) is detected. It's recommended to set this bit to "1" after the battery pack is assembled.

Bit6 (T1E): Enable the first external temperature sensor (THERM1) check in Hardware Mode. In Hardware Mode, if this bit is "1", the first external temperature will be checked; if this bit is "0", the first external temperature will not be checked. In Software Mode, this bit is ignored.

Bit7 (T2E): Enable the second external temperature sensor (THERM2) check in Hardware Mode. In Hardware Mode, if "1", enable to check the second external temperature; if "0", disable to check the second external temperature. In Software Mode, this bit is ignored.

==========

EEPROM Register 33h – Hardware Bleeding Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UC1	UC0	SS	PS	BS	SEB	BCNC1	BCNC0

Bit1 – Bit0 (BCNC1 – BCNC0): Specify the maximum number of simultaneously bleeding cells for external bleeding. If internal bleeding is selected, these two bits are ignored, always just bleed the highest cell.

BCNC1 – BCNC0	Maximum bleeding cell number
00	1
01	2
10	3
11	4

Bit2 (SEB): Select external bleeding or internal bleeding. If "1", select external bleeding function; if "0", select internal bleeding.

Bit3 (BS): Enable bleeding function if set to "1", otherwise disabled.

Bit4 (PS): Enable pre-charge function if set to "1", otherwise disabled.

Bit5 (SS): Enable the sleep mode if set to "1". Otherwise, can't enter sleep mode.

Bit7 – Bit6 (UC1 – UC0): Control access to EEPROM user data section to protect data from accidental modification and ADC Safety scan enable/disable

UC1 – UC0	Safety scan, access to user data
00	The ADC safety scan is disabled; can read/write user data section
01	The ADC safety scan is enabled; can read/write user data section
10	The ADC safety scan is enabled; can read user data section but cannot write user data section.
11	The ADC safety scan is enabled; cannot read/write user data section.

==========

EEPROM Register 34h – Sense Resistor Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0

This register is used to store the sense resistor value. It is unsigned value N: if N = 0, the sense resistor value is 2.5mohm, if N ≠ 0, the sensor resistor value is N*0.1 mohm.

EEPROM Register 36h ~ 3fh – Factory Name Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FN7	FN6	FN5	FN4	FN3	FN2	FN1	FN0

These 10 registers (10-byte) store user factory name (ASCII code). Name length can be up to 10 characters.

EEPROM Register 40h ~ 44h – Project Name Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PN7	PN6	PN5	PN4	PN3	PN2	PN1	PN0

These 5 registers (5-byte) store user project name (ASCII code). Name length can be up to 5 characters.

EEPROM Register 45h – Version Number Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VNR7	VNR6	VNR5	VNR4	VNR3	VNR2	VNR1	VNR0

This register (1-byte) stores user version number.

==========

EEPROM Register 46h/47h – Cell Unbalance Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
46h	CUT4	CUT3	CUT2	CUT1	CUT0	reserved	reserved	reserved
47h	CUT12	CUT11	CUT10	CUT9	CUT8	CUT7	CUT6	CUT5

CUT12 – CUT0: Specify the cell unbalanced threshold voltage ***PFCUTH*** as N * 1.22mv (N is 13-bit signed value). If the voltage difference between highest cell and lowest cell exceeds this threshold, OZ890 will generate PF signal. To disable this PF function, just fill a very large voltage value in these two registers.

==========

EEPROM Register 48h/49h – Bleeding Start Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
48h	BSV4	BSV3	BSV2	BSV1	BSV0	BA2	BA1	BA0
49h	BSV12	BSV11	BSV10	BSV9	BSV8	BSV7	BSV6	BSV5

These 2 registers set the bleeding start voltage and bleeding accuracy. Refer to "Internal/External Bleeding" section for detail.

Bit2 – Bit0 (BA2 – BA0): Specify the bleeding accuracy.

BA2 – BA0	Bleeding Accuracy
000	8*1.22 = 9.76mv
001	16*1.22 = 19.5mv
010	24*1.22 = 29.3mv
011	32*1.22 = 39.0mv
100	40*1.22 = 48.80mv
101	48*1.22 = 58.56mv
110	56*1.22 = 68.3mv
111	64*1.22 = 78.1mv

The cell bleeding will be disabled if the Vcell_max – Vcell_min < bleeding accuracy.

BSV12 – BSV0: Specify the bleeding start voltage as N*1.22mv (N is 13-bit signed value).

==========

EEPROM Register 4ah/4bh – OV Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4ah	OVT4	OVT3	OVT2	OVT1	OVT0	reserved	reserved	reserved
4bh	OVT12	OVT11	OVT10	OVT9	OVT8	OVT7	OVT6	OVT5

OVT12 – OVT0: Specify the OV threshold voltage as N*1.22mv (N is 13-bit signed value).

==========

EEPROM Register 4ch/4dh – OV Release Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4ch	OVR4	OVR3	OVR2	OVR1	OVR0	reserved	reserved	reserved
4dh	OVR12	OVR11	OVR10	OVR9	OVR8	OVR7	OVR6	OVR5

OVR12 – OVR0: Specify the OV release voltage as N*1.22mv (N is 13-bit signed value). User should set this OV release voltage lower than OV threshold voltage.

==========

EEPROM Register 4eh/4fh – UV Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4eh	UVT4	UVT3	UVT2	UVT1	UVT0	reserved	reserved	reserved
4fh	UVT12	UVT11	UVT10	UVT9	UVT8	UVT7	UVT6	UVT5

UVT12 – UVT0: Specify the UV threshold voltage as N*1.22mv (N is 13-bit signed value).

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EEPROM Register 50h/51h – UV Release Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50h	UVR4	UVR3	UVR2	UVR1	UVR0	reserved	reserved	reserved
51h	UVR12	UVR11	UVR10	UVR9	UVR8	UVR7	UVR6	UVR5

UVR12 – UVR0: Specify the UV release voltage as N*1.22mv (N is 13-bit signed value). User should set this UV release voltage higher than UV threshold voltage.

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EEPROM Register 52h/53h – Extremely High Voltage Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	PFVH4	PFVH3	PFVH2	PFVH1	PFVH0	reserved	reserved	reserved
53h	PFVH12	PFVH11	PFVH10	PFVH9	PFVH8	PFVH7	PFVH6	PFVH5

PFVH12 – PFVH0: Specify the extremely high voltage threshold ***PFVHTH*** as N*1.22mv (N is 13-bit signed value).

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EEPROM Register 54h/55h – Extremely Low Voltage Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54h	PFVL4	PFVL3	PFVL2	PFVL1	PFVL0	reserved	reserved	reserved
55h	PFVL12	PFVL11	PFVL10	PFVL9	PFVL8	PFVL7	PFVL6	PFVL5

PFVL12 – PFVH0: Specify the extremely low voltage threshold ***PFVLTH*** as N*1.22mv (N is 13-bit signed value).

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EEPROM Register 56h/57h – OTE Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
56h	OTET4	OTET3	OTET2	OTET1	OTET0	reserved	reserved	reserved
57h	OTET12	OTET11	OTET10	OTET9	OTET8	OTET7	OTET6	OTET5

OTET12 – OTET0: Specify the 1 external over temperature threshold voltage as N*0.61mv (N is 13-bit signed value). Please refer to “External Temperature Sensor” section.

EEPROM Register 58h/59h – OTE Release Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
58h	OTER4	OTER3	OTER2	OTER1	OTER0	reserved	reserved	reserved
59h	OTER12	OTER11	OTER10	OTER9	OTER8	OTER7	OTER6	OTER5

OTER12 – OTER0: Specify the external over temperature release voltage as N*0.61mv (N is 13-bit signed value). Please refer to “External Temperature Sensor” section.
==========

EEPROM Register 5ah/5bh – UTE Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5ah	UTET4	UTET3	UTET2	UTET1	UTET0	reserved	reserved	reserved
5bh	UTET12	UTET11	UTET10	UTET9	UTET8	UTET7	UTET6	UTET5

UTET12 – UTET0: Specify the external under temperature threshold voltage as N*0.61mv (N is 13-bit signed value). Please refer to “External Temperature Sensor” section.

EEPROM Register 5ch/5dh – UTE Release Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5ch	UTER4	UTER3	UTER2	UTER1	UTER0	reserved	reserved	reserved
5dh	UTER12	UTER11	UTER10	UTER9	UTER8	UTER7	UTER6	UTER5

UTER12 – UTER0: Specify the external under temperature release voltage as N*0.61mv (N is 13-bit signed value). Please refer to “External Temperature Sensor” section.
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EEPROM Register 5eh/5fh – OTI Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5eh	OTIT4	OTIT3	OTIT2	OTIT1	OTIT0	reserved	reserved	reserved
5fh	OTIT12	OTIT11	OTIT10	OTIT9	OTIT8	OTIT7	OTIT6	OTIT5

OTIT12 – OTIT0: Specify the internal over temperature threshold voltage as N*0.61mv (N is 13-bit signed value). Please refer to “Internal Temperature Sensor” section.

EEPROM Register 60h/61h – OTI Release Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
60h	OTIR4	OTIR3	OTIR2	OTIR1	OTIR0	reserved	reserved	reserved
61h	OTIR12	OTIR11	OTIR10	OTIR9	OTIR8	OTIR7	OTIR6	OTIR5

OTIR12 – OTIR0: Specify the internal over temperature release voltage as N*0.61mv (N is 13-bit signed value). Please refer to “Internal Temperature Sensor” section.
==========

EEPROM Register 62h/63h – UTI Threshold Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
62h	UTIT4	UTIT3	UTIT2	UTIT1	UTIT0	reserved	reserved	reserved
63h	UTIT12	UTIT11	UTIT10	UTIT9	UTIT8	UTIT7	UTIT6	UTIT5

UTIT12 – UTIT0: Specify the internal under temperature threshold voltage as N*0.61mv (N is 13-bit signed value). Please refer to “Internal Temperature Sensor” section.

EEPROM Register 64h/65h – UTI Release Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
64h	UTIR4	UTIR3	UTIR2	UTIR1	UTIR0	reserved	reserved	reserved
65h	UTIR12	UTIR11	UTIR10	UTIR9	UTIR8	UTIR7	UTIR6	UTIR5

UTIR12 – UTIR0: Specify the internal under temperature release voltage as N*0.61mv (N is 13-bit signed value). Please refer to “Internal Temperature Sensor” section.

==========

EEPROM Register 66h/67h – Gas Gauge V1 Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
66h	GGVA4	GGVA3	GGVA2	GGVA1	GGVA0	reserved	reserved	reserved
67h	GGVA12	GGVA11	GGVA10	GGVA9	GGVA8	GGVA7	GGVA6	GGVA5

GGVA12 – GGVA0: Specify the Gauge V1 voltage as N*1.22mv (N is 13-bit signed value). Please refer to “Voltage Based Gas Gauge” section.

EEPROM Register 68h/69h – Gas Gauge V2 Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
68h	GGVB4	GGVB3	GGVB2	GGVB1	GGVB0	reserved	reserved	reserved
69h	GGVB12	GGVB11	GGVB10	GGVB9	GGVB8	GGVB7	GGVB6	GGVB5

GGVB12 – GGVB0: Specify the Gauge V2 voltage as N*1.22mv (N is 13-bit signed value). Please refer to “Voltage Based Gas Gauge” section.

EEPROM Register 6ah/6bh – Gas Gauge V3 Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6ah	GGVC4	GGVC3	GGVC2	GGVC1	GGVC0	reserved	reserved	reserved
6bh	GGVC12	GGVC11	GGVC10	GGVC9	GGVC8	GGVC7	GGVC6	GGVC5

GGVC12 – GGVC0: Specify the Gauge V3 voltage as N*1.22mv (N is 13-bit signed value). Please refer to “Voltage Based Gas Gauge” section.

EEPROM Register 6ch/6dh – Gas Gauge V4 Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6ch	GGVD4	GGVD3	GGVD2	GGVD1	GGVD0	reserved	reserved	reserved
6dh	GGVD12	GGVD11	GGVD10	GGVD9	GGVD8	GGVD7	GGVD6	GGVD5

GGVD12 – GGVD0: Specify the Gauge V4 voltage as N*1.22mv (N is 13-bit signed value). Please refer to “Voltage Based Gas Gauge” section.

EEPROM Register 6eh/6fh – Gas Gauge V5 Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6eh	GGVE4	GGVE3	GGVE2	GGVE1	GGVE0	reserved	reserved	reserved
6fh	GGVE12	GGVE11	GGVE10	GGVE9	GGVE8	GGVE7	GGVE6	GGVE5

GGVE12 – GGVE0: Specify the Gauge V5 voltage as N*1.22mv (N is 13-bit signed value). Please refer to “Voltage Based Gas Gauge” section.

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EEPROM Register 7ah/7bh – Password Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7ah	PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0
7bh	PWD15	PWD14	PWD13	PWD12	PWD11	PWD10	PWD9	PWD8

PWD15 – PWD0: Specify the 16-bit customer password to enable EEPROM block erase. Please refer to “Password Verification Function” section.

EEPROM Register 7ch/7dh – Authentication Code Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

7ch	ATHC7	ATHC6	ATHC5	ATHC4	ATHC3	ATHC2	ATHC1	ATHC0
7dh	ATHC15	ATHC14	ATHC13	ATHC12	ATHC11	ATHC10	ATHC9	ATHC8

ATHC15 – ATHC0: Specify the 16-bit authentication code (seed) for OZ890 internal CRC algorithm. Please refer to “Authentication” section.

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EEPROM Register 7fh – Authentication Control Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7fh	STFRZ	reserved	reserved	reserved	reserved	reserved	ATHCC1	ATHCC0

Bit1 – Bit0 (ATHCC1 – ATHCC0): Specify the authentication scope.

ATHCC1 – ATHCC0	Description
00	Disable charge authentication Disable discharge authentication
01	Enable charge authentication Disable discharge authentication
10	Disable charge authentication Enable discharge authentication
11	Enable charge authentication Enable discharge authentication

Bit7 (STFRZ): Freeze the EEPROM secret_data section if set to “1”.

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Operation Registers

OZ890 Operation Registers store the instant ADC readings, OZ890 chip status information, etc. They also provide the control registers to control OZ890's operation.

Operation Registers Map

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
00h	Chip ID & Chip Revision	CHP_ID3	CHP_ID2	CHP_ID1	CHP_ID0	CHP_REV3	CHP_REV2	CHP_REV1	CHP_REV0
01h~05h	Reserved	reserved							
06h	Cell Number	NIMH_ VPKOL	reserved	BTYP1	BTYP0	CNUM3	CNUM2	CNUM1	CNUM0
07h	Scan Rate	NO_SNSR	SCN_RT2	SCN_RT1	SCN_RT0	reserved	EFETC_ SHDN_ ENB	EFETC1	EFETC0
08h	OC Charge Control	DCTC2	DCTC1	DCTC0	OCCFC4	OCCFC3	OCCFC2	OCCFC1	OCCFC0
09h	OC Discharge Control	CCTC1	CCTC0	OCCFD5	OCCFD4	OCCFD3	OCCFD2	OCCFD1	OCCFD0
0ah	OC Delay	OCDN4	OCDN3	OCDN2	OCDN1	OCDN0	OCDS2	OCDS1	OCDS0
0bh	SC Control	reserved	reserved	SCC5	SCC4	SCC3	SCC2	SCC1	SCC0
0ch	SC Delay	SCDN4	SCDN3	SCDN2	SCDN1	SCDN0	SCDS2	SCDS1	SCDS0
0dh	OC Release Control	NO_ER_ DSPL	IDL_BLD_ ENB	DOCRC2	DOCRC1	DOCRC0	COCRC2	COCRC1	COCRC0
0eh	OT/UT, OV/UV Delay Control	OTUTD3	OTUTD2	OTUTD1	OTUTD0	OVUVD3	OVUVD2	OVUVD1	OVUVD0
0fh	PF Control	reserved	MFPF_ENB	VHPF_ENB	VLPF_ENB	PFD3	PFD2	PFD1	PFD0
10h	I2C Address Config and SC Release Control	SCRC2	SCRC1	SCRC0	PEC_ENB	I2CADDR3	I2CADDR2	I2CADDR1	I2CADDR0
11h	Wake Up Control	reserved	reserved	reserved	reserved	SLP_T3	SLP_T2	SLP_T1	SLP_T0
12h	Mode Control	T2E	T1E	RSTN_ BYPASS	reserved	V_OFF_ DIS	I_OFF_DI S	BLD_AL L_EN	HM
13h	Hardware Bleeding	UC1	UC0	SS	PS	BS	SEB	BCNC1	BCNC0
14h	Software Sleep Control	reserved	reserved	reserved	LOW_ PW_ST	SLP_ EXP_EVT	reserved	WC_WK_ EVT	SLP_REQ
15h	Shut Down	reserved	reserved	reserved	CUPF_EVT	MFPF_EVT	VHPF_EVT	VLPF_EVT	SHDW_REQ
16h	OV/UV timer	reserved	reserved	reserved	reserved	OVUV_TM3	OVUV_TM2	OVUV_TM1	OVUV_TM0
17h	reserved	reserved							
18h	OC Timer	OCTM7	OCTM6	OCTM5	OCTM4	OCTM3	OCTM2	OCTM1	OCTM0
19h	PF timer	reserved	reserved	PFTM5	PFTM4	PFTM3	PFTM2	PFTM1	PFTM0

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
1ah	Deadman Control	reserved	reserved	reserved	reserved	DMN_RST_ ENB	DMN_C2	DMN_C1	DMN_C0
1bh	Deadman Timer	reserved	CLR_TM	DMN_TM5	DMN_TM4	DMN_TM3	DMN_TM2	DMN_TM1	DMN_TM0
1ch	Check Yes	OT_YES	UT_YES	OV_YES	CUPF_YES	MFPF_YES	VHPF_YES	VLPF_YES	UV_YES
1dh	PWM Discharge	reserved	reserved	PWM_FC1	PWM_FC0	PWM_DC3	PWM_DC2	PWM_DC1	PWM_DC0
1eh	FET Enable	reserved	reserved	reserved	reserved	reserved	PCHG_ENB	CHG_ENB	DSG_ENB
1fh	FET Disable	reserved	reserved	UT_DSBL	OT_DSBL	SC_DSBL	OC_DSBL	UV_DSBL	OV_DSBL
20h	Charge/ Discharge State	reserved	reserved	reserved	reserved	CHG_ST	DSG_ST	reserved	reserved
21h	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
22h	Software Bleeding	BLD_CL7	BLD_CL6	BLD_CL5	BLD_CL4	BLD_CL3	BLD_CL2	BLD_CL1	BLD_CL0
23h		TCLK_F1	TCLK_F0	BLD_ENB	BLD_CL12	BLD_CL11	BLD_CL10	BLD_CL9	BLD_CL8
24h	ADC Request	ADC_RES1	ADC_RES0	ADC_CH5	ADC_CH4	ADC_CH3	ADC_CH2	ADC_CH1	ADC_CH0
25h	ADC Busy	ADC_RES1	ADC_RES0	reserved	reserved	reserved	reserved	reserved	ADC_BUSY
26h	ADC Data	ADC_D7	ADC_D6	ADC_D5	ADC_D4	ADC_D3	ADC_D2	ADC_D1	ADC_D0
27h		ADC_D15	ADC_D14	ADC_D13	ADC_D12	ADC_D11	ADC_D10	ADC_D9	ADC_D8
28h	OT/UT Timer	G2_OTUT3	G2_OTUT2	G2_OTUT1	G2_OTUT0	G1_OTUT3	G1_OTUT2	G1_OTUT1	G1_OTUT0
29h		IT_OTUT3	IT_OTUT2	IT_OTUT1	IT_OTUT0	G3_OTUT3	G3_OTUT2	G3_OTUT1	G3_OTUT0
2ah	Event Enable	SCN_EVT_ ENB	ADC_EVT _ENB	UT_EVT_ ENB	OT_EVT_ ENB	SC_EVT_ ENB	OC_EVT_ ENB	UV_EVT_ ENB	OV_EVT_ ENB
2bh	Event	SCN_EVT	ADC_EVT	UT_EVT	OT_EVT	SC_EVT	OC_EVT	UV_EVT	OV_EVT
2ch	1S timer	reserved	SC_RLS	TM1S5	TM1S4	TM1S3	TM1S2	TM1S1	TM1S0
2dh	GPIO Mode	G3_MD1	G3_MD0	G3_RES1	G3_RES0	G2_MD1	G2_MD0	G1_MD1	G1_MD0
2eh	GP Event & Data	G3_EVT	G2_EVT	G1_EVT	G0_EVT	G3_IN	G2_IN	G1_IN	G0_IN
2fh	GP Event Enable	G3_EVT_ ENB	G2_EVT_ ENB	G1_EVT_ ENB	G0_EVT_ _ENB	reserved	reserved	reserved	reserved
30h	GPO Enable & Data	G3_OUT_ ENB	G2_OUT_ ENB	G1_OUT_ ENB	G0_OUT_ _ENB	G3_OUT	G2_OUT	G1_OUT	G0_OUT
31h	reserved	reserved							
32h	Cell 1 ADC Data	CELL1_D4	CELL1_D3	CELL1_D2	CELL1_D1	CELL1_D0	reserved	reserved	reserved
33h		CELL1_D12	CELL1_D11	CELL1_D10	CELL1_D9	CELL1_D8	CELL1_D7	CELL1_D6	CELL1_D5
34h	Cell 2 ADC Data	CELL2_D4	CELL2_D3	CELL2_D2	CELL2_D1	CELL2_D0	reserved	reserved	reserved
35h		CELL2_D12	CELL2_D11	CELL2_D10	CELL2_D9	CELL2_D8	CELL2_D7	CELL2_D6	CELL2_D5
36h	Cell 3 ADC Data	CELL3_D4	CELL3_D3	CELL3_D2	CELL3_D1	CELL3_D0	reserved	reserved	reserved
37h		CELL3_D12	CELL3_D11	CELL3_D10	CELL3_D9	CELL3_D8	CELL3_D7	CELL3_D6	CELL3_D5
38h	Cell 4 ADC Data	CELL4_D4	CELL4_D3	CELL4_D2	CELL4_D1	CELL4_D0	reserved	reserved	reserved
39h		CELL4_D12	CELL4_D11	CELL4_D10	CELL4_D9	CELL4_D8	CELL4_D7	CELL4_D6	CELL4_D5
3ah	Cell 5 ADC Data	CELL5_D4	CELL5_D3	CELL5_D2	CELL5_D1	CELL5_D0	reserved	reserved	reserved
3bh		CELL5_D12	CELL5_D11	CELL5_D10	CELL5_D9	CELL5_D8	CELL5_D7	CELL5_D6	CELL5_D5
3ch	Cell 6 ADC Data	CELL6_D4	CELL6_D3	CELL6_D2	CELL6_D1	CELL6_D0	reserved	reserved	reserved
3dh		CELL6_D12	CELL6_D11	CELL6_D10	CELL6_D9	CELL6_D8	CELL6_D7	CELL6_D6	CELL6_D5
3eh	Cell 7	CELL7_D4	CELL7_D3	CELL7_D2	CELL7_D1	CELL7_D0	reserved	reserved	reserved

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
3fh	ADC Data	CELL7_D12	CELL7_D11	CELL7_D10	CELL7_D9	CELL7_D8	CELL7_D7	CELL7_D6	CELL7_D5
40h	Cell 8 ADC Data	CELL8_D4	CELL8_D3	CELL8_D2	CELL8_D1	CELL8_D0	reserved	reserved	reserved
41h		CELL8_D12	CELL8_D11	CELL8_D10	CELL8_D9	CELL8_D8	CELL8_D7	CELL8_D6	CELL8_D5
42h	Cell 9 ADC Data	CELL9_D4	CELL9_D3	CELL9_D2	CELL9_D1	CELL9_D0	reserved	reserved	reserved
43h		CELL9_D12	CELL9_D11	CELL9_D10	CELL9_D9	CELL9_D8	CELL9_D7	CELL9_D6	CELL9_D5
44h	Cell 10 ADC Data	CELL10_D4	CELL10_D3	CELL10_D2	CELL10_D1	CELL10_D0	reserved	reserved	reserved
45h		CELL10_D12	CELL10_D11	CELL10_D10	CELL10_D9	CELL10_D8	CELL10_D7	CELL10_D6	CELL10_D5
46h	Cell 11 ADC Data	CELL11_D4	CELL11_D3	CELL11_D2	CELL11_D1	CELL11_D0	reserved	reserved	reserved
47h		CELL11_D12	CELL11_D11	CELL11_D10	CELL11_D9	CELL11_D8	CELL11_D7	CELL11_D6	CELL11_D5
48h	Cell 12 ADC Data	CELL12_D4	CELL12_D3	CELL12_D2	CELL12_D1	CELL12_D0	reserved	reserved	reserved
49h		CELL12_D12	CELL12_D11	CELL12_D10	CELL12_D9	CELL12_D8	CELL12_D7	CELL12_D6	CELL12_D5
4ah	Cell 13 ADC Data	CELL13_D4	CELL13_D3	CELL13_D2	CELL13_D1	CELL13_D0	reserved	reserved	reserved
4bh		CELL13_D12	CELL13_D11	CELL13_D10	CELL13_D9	CELL13_D8	CELL13_D7	CELL13_D6	CELL13_D5
4ch	GPIO1 ADC Data	GPIO1_D4	GPIO1_D3	GPIO1_D2	GPIO1_D1	GPIO1_D0	reserved	reserved	reserved
4dh		GPIO1_D12	GPIO1_D11	GPIO1_D10	GPIO1_D9	GPIO1_D8	GPIO1_D7	GPIO1_D6	GPIO1_D5
4eh	GPIO2 ADC Data	GPIO2_D4	GPIO2_D3	GPIO2_D2	GPIO2_D1	GPIO2_D0	reserved	reserved	reserved
4fh		GPIO2_D12	GPIO2_D11	GPIO2_D10	GPIO2_D9	GPIO2_D8	GPIO2_D7	GPIO2_D6	GPIO2_D5
50h	GPIO3 ADC Data	GPIO3_D7	GPIO3_D6	GPIO3_D5	GPIO3_D4	GPIO3_D3	GPIO3_D2	GPIO3_D1	GPIO3_D0
51h		GPIO3_D15	GPIO3_D14	GPIO3_D13	GPIO3_D12	GPIO3_D11	GPIO3_D10	GPIO3_D9	GPIO3_D8
52h	INT ADC Data	INT_D4	INT_D3	INT_D2	INT_D1	INT_D0	reserved	reserved	reserved
53h		INT_D12	INT_D11	INT_D10	INT_D9	INT_D8	INT_D7	INT_D6	INT_D5
54h	Current ADC Data	CRRT_D7	CRRT_D6	CRRT_D5	CRRT_D4	CRRT_D3	CRRT_D2	CRRT_D1	CRRT_D0
55h		CRRT_D15	CRRT_D14	CRRT_D13	CRRT_D12	CRRT_D11	CRRT_D10	CRRT_D9	CRRT_D8
56h	Group1 Offset	GRP1_OST7	GRP1_OST6	GRP1_OST5	GRP1_OST4	GRP1_OST3	GRP1_OST2	GRP1_OST1	GRP1_OST0
57h	Group2 Offset	GRP2_OST7	GRP2_OST6	GRP2_OST5	GRP2_OST4	GRP2_OST3	GRP2_OST2	GRP2_OST1	GRP2_OST0
58h	Group3 Offset	GRP3_OST7	GRP3_OST6	GRP3_OST5	GRP3_OST4	GRP3_OST3	GRP3_OST2	GRP3_OST1	GRP3_OST0
59h	GPIO Offset	GP_OST7	GP_OST6	GP_OST5	GP_OST4	GP_OST3	GP_OST2	GP_OST1	GP_OST0
5ah	Current Offset	CRRT_OST7	CRRT_OST6	CRRT_OST5	CRRT_OST4	CRRT_OST3	CRRT_OST2	CRRT_OST1	CRRT_OST0
5bh		reserved	reserved	reserved	reserved	CRRT_OST11	CRRT_OST10	CRRT_OST9	CRRT_OST8
5ch	EEPROM Data	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
5dh		EE_D15	EE_D14	EE_D13	EE_D12	EE_D11	EE_D10	EE_D9	EE_D8
5eh	EEPROM Address	reserved	EE_ADDR6	EE_ADDR5	EE_ADDR4	EE_ADDR3	EE_ADDR2	EE_ADDR1	EE_ADDR0
5fh	EEPROM Control	EE_BUSY	EE_MD2	EE_MD1	EE_MD0	EE_CODE3	EE_CODE2	EE_CODE1	EE_CODE0
60h~68h	Reserved	reserved							
69h	Password	PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0
6ah		PWD15	PWD14	PWD13	PWD12	PWD11	PWD10	PWD9	PWD8
6bh	Authentication Random Number	ATH_NM7	ATH_NM6	ATH_NM5	ATH_NM4	ATH_NM3	ATH_NM2	ATH_NM1	ATH_NM0
6ch		ATH_NM15	ATH_NM14	ATH_NM13	ATH_NM12	ATH_NM11	ATH_NM10	ATH_NM9	ATH_NM8
6dh	Authentication Data	ATH_D7	ATH_D6	ATH_D5	ATH_D4	ATH_D3	ATH_D2	ATH_D1	ATH_D0
6eh		ATH_D15	ATH_D14	ATH_D13	ATH_D12	ATH_D11	ATH_D10	ATH_D9	ATH_D8
6fh	Password/ Authentication Status	PWD_FAIL	PWD_OK	PWD_BUSY	reserved	ATH_DSG_ FAIL	ATH_DSG_ OK	ATH_CHG_ FAIL	ATH_CHG_ OK

Register index (hex)	Register Name	Bit Number							
		7	6	5	4	3	2	1	0
70h~7bh	Reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
7ch	Authentication Code	ATHC7	ATHC6	ATHC5	ATHC4	ATHC3	ATHC2	ATHC1	ATHC0
7dh		ATHC15	ATHC14	ATHC13	ATHC12	ATHC11	ATHC10	ATHC9	ATHC8
7eh	Reserved	reserved							
7fh	Authentication Control	STFRZ	reserved	reserved	reserved	reserved	reserved	ATHCC1	ATHCC0

Detailed Operation Registers Information

Register 00h – Chip ID & Revision Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CHP_ID3 (R)	CHP_ID2 (R)	CHP_ID1 (R)	CHP_ID0 (R)	CHP_REV3 (R)	CHP_REV2 (R)	CHP_REV1 (R)	CHP_REV0 (R)

Default value is 8'h02.

Bit7 – Bit4 (CHP_ID3 – CHP_ID0) is chip ID (4'h0) indicating OZ890.

Bit3 – Bit0 (CHP_REV3 – CHP_REV0) is chip revision (4'h2) indicating C version.

==========

Register 06h ~ 13h

Operation Registers 06h ~ 13h are mapped from EEPROM Registers 26h ~ 33h during EEPROM mapping. (During power up sequence, it will automatically do an EEPROM mapping operation one time). Please refer to "Detailed EEPROM Registers information" section for detailed register definition.

When UC1 – UC0 (Bit7 – Bit6 in Operation Register 13h) is 2'b00 or 2'b01, Operation Registers 06h ~ 13h can be modified via the I2C interface. Note HM (Bit 0 in Operation Register 13h) is R (read-only) which cannot be written with I2C interface. User can test effects of the parameters with this function before writing the parameters into the EEPROM.

When UC1 – UC0 (Bit7 – Bit6 in Operation Register 13h) is 2'b10 or 2'b11, Operation Registers 06h ~ 13h are R (read only) so that I2C interface cannot modify them to prevent from unexpected change.

==========

Register 14h – Software Sleep Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	reserved	LOW_PW_ST (R)	SLP_EXP_EVT	reserved	SC_WK_EVT	SLP_REQ

Default value is 8'h0.

Bit4 (LOW_PW_ST): If "1", indicate that OZ890 is running in low power state.

Bit3 (SLP_EXP_EVT): When OZ890 is woken up by sleep timer, this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit.

Bit1 (WC_WK_EVT): When OZ890 is woken up by SC(short circuit), this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit.

Bit0 (SLP_REQ): Request OZ890 to enter sleep mode in software mode by writing "1" into this bit. When this bit is "1", if no OV, OC, SC, OT, UT, VHPF, VLPF event, OZ890 will enter sleep mode; if any of these events occurs, OZ890 will stay in full power mode even though this bit is set to "1".
In hardware mode, this bit is ignored.

If any of SLP_EXP_EVT, SC_WK_EVT is set to "1", the ALERTN pin will be active to inform the external Microprocessor.

==========

Register 15h – Shut Down Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	reserved	CUPF_EVT	MFPF_EVT	VHPF_EVT	VLPF_EVT	_SHDW_REQ

Default value is 8'h0.

Bit4 (CUPF_EVT): When the cell unbalance event is detected, this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit.

Bit3 (MFPF_EVT): When the mosfet failure event is detected, this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit.

Bit2 (VHPF_EVT): When the VHPF event is detected, this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit.

Bit1 (VLPF_EVT): When the VLPF event is detected, this bit will be set to "1" and be kept until the software clears it by writing "1" into this bit.

Bit0 (SHDW_REQ): Request OZ890 to enter shut down mode by writing "1" into this bit in software mode or hardware mode.

==========

Register 16h – OV/UV Timer Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	reserved	reserved	OVUV_TM3 (R)	OVUV_TM2 (R)	OVUV_TM1 (R)	OVUV_TM0 (R)

Default value is 8'h0.

Bit3 – Bit0 (OVUV_TM3 – OVUV_TM0): the timer for the OV/UV delay or OV/UV release. Its unit is a scan cycle (in normal case, it is 1second).

==========

Register 18h – OC Timer Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCTM7 (R)	OCTM6 (R)	OCTM5 (R)	OCTM4 (R)	OCTM3 (R)	OCTM2 (R)	OCTM1 (R)	OCTM0 (R)

Default value is 8'h0.

Bit7 – Bit0 (OCTM7 – OCTM0): the timer for the OC delay or OC release. For OC delay, its unit is OC delay unit defined in OC Delay register; for OC release, its unit is 0.2s second.

==========

Register 19h – PF Timer Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	PFTM5 (R)	PFTM4 (R)	PFTM3 (R)	PFTM2 (R)	PFTM1 (R)	PFTM0 (R)

Default value is 8'h0.

Bit5 – Bit0 (PFTM5 – PFTM0): the timer for the Permanent Failure event. Its unit is a scan cycle (in normal case, it is 1 second).

==========

Register 1ah – Deadman Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	reserved	reserved	DMN_RST_ ENB	DMN_C2	DMN_C1	DMN_C0

Register 1ah and 1bh are used to control the deadman detection. Refer to "Deadman PF (DMPF)" Section for detail.

Default value is 8'h0.

Bit3 (DMN_RST_ENB): Enable reset function when the deadman is detected. If “1”, the chip will assert a low active pulse to the RSTN pin to reset the external Microprocessor when the deadman event occurs; if “0”, the chip will turn off all MOSFETs and enter shut down mode when the deadman event occurs.

Bit2 – Bit0 (DMN_C2 – DMN_C0): Control the deadman time as follows:

DMN_C2 – DMN_C0	**Allowed Max Deadman Time**
000	Infinite(deadman check is disabled)
001	3 seconds
010	7 seconds
011	15 seconds
100	31 seconds
>=101	63 seconds

==========

Register 1bh – Deadman Timer Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	CLR_TM	DMN_TM5 (R)	DMN_TM4 (R)	DMN_TM3 (R)	DMN_TM2 (R)	DMN_TM1 (R)	DMN_TM0 (R)

Default value is 8’h0.

Bit6 (CLR_TM): Clear the deadman timer by writing “1” into this bit. When this bit is read-out, it always is “0”.

Bit5 – Bit0 (DMN_TM5 – DMN_TM0): the deadman timer with 1s unit.

==========

Register 1ch – Check Yes Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OT_YES (R)	UT_YES (R)	OV_YES (R)	CUPF_YES (R)	MFPF_YES (R)	VHPF_YES (R)	VLPF_YES (R)	UV_YES (R)

Default value is 8’h0.

Bit7 (OT_YES): If “1”, OT (Over Temperature) is detected.

Bit6 (UT_YES): If “1”, UT (Under Temperature) is detected.

Bit5 (OV_YES): If “1”, OV (Over Voltage) is detected.

Bit4 (CUPF_YES): If “1”, CUPF (Cell Unbalance Permanente Fail) is detected.

Bit3 (MFPF_YES): If “1”, CUPF (MOSFET Permanente Fail) is detected.

Bit2 (VHPF_YES): If “1”, VHPF (Cell Voltage Extremely High Permanente Fail) is detected.

Bit1 (VLPF_YES): If “1”, VLPF (Cell Voltage Extremely Low Permanente Fail) is detected.

Bit0 (UV_YES): If “1”, UV (Under Voltage) is detected.

==========

Register 1dh – PWM Discharge Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	PWM_FC1	PWM_FC0	PWM_DC3	PWM_DC2	PWM_DC1	PWC_DC0

Default value is 8'h1f. This register is used to control PWM discharge in software mode. In hardware mode, this register is ignored.

Bit5 – Bit4 (PWM_FC1 – PWM_FC0): Specify the frequency for PWM discharge in software mode as follows:

PWM_FC1 – PWM_FC0	Frequency for PWM Discharge
2'b00	1khz
2'b01(Default)	2khz
2'b10	4khz
2'b11	8khz

Bit3 – Bit0 (PWM_DC3 – PWM_DC0): Specify the duty for PWM discharge in software mode as follows:

PWM_DC3 – PWM_DC0	Duty (high active) for PWM Discharge
4'b0000	Always low(full off)
4'b0001	18.8%
4'b0010	25%
4'b0011	31.3%
4'b0100	137.5%
4'b0101	43.8%
4'b0110	50%
4'b0111	56.3%
4'b1000	62.5%
4'b1001	68.8%
4'b1010	75%
4'b1011	81.3%
4'b1100	87.5%
4'b1101	93.8%
4'b1110	96.9%
4'b1111 (Default)	100% (full on)

==========

Register 1eh – FET Enable Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	reserved	reserved	reserved	PCHG_ENB	CHG_ENB	DSG_ENB

Default value is 8'h0. This register is used to forcedly turn off the MOSFETs in software mode. In hardware mode, this register is ignored.

Bit2 (PCHG_ENB): If "0", forcedly turn off the precharge MOSFET; if "1", the precharge MOSFET is decided by the safety check.

Bit1 (CHG_ENB): If "0", forcedly turn off the charge MOSFET; if "1", the charge MOSFET is decided by the safety check.

Bit0 (DSG_ENB): If "0", forcedly turn off the discharge MOSFET; if "1", the discharge MOSFET is decided by the safety check.

==========

Register 1fh – FET Disable Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	UT_DSBL	OT_DSBL	SC_DSBL	OC_DSBL	UV_DSBL	OV_DSBL

Default value is 8'h0. In hardware mode, this register is R (Read-Only). In software mode, this register is RW (Read/Write), the software can clear the corresponding bit by writing "1" into it.

Bit5 (UT_DSBL): This bit is set to "1" when the time of UT equals to UT delay. In hardware mode, this bit will be kept "1" until UT release; in software mode, this bit will be kept "1" until software clears it by writing "1" into this bit.

Bit4 (OT_DSBL): This bit is set to “1” when the time of OT equals to OT delay. In hardware mode, this bit will be kept “1” until OT release; in software mode, this bit will be kept “1” until software clears it by writing “1” into this bit.

Bit3 (SC_DSBL): This bit is set to “1” when the time of SC equals to SC delay. In hardware mode, this bit will be kept “1” until SC release; in software mode, this bit will be kept “1” until software clears it by writing “1” into this bit.

Bit2 (OC_DSBL): This bit is set to “1” when the time of OC equals to OC delay. In hardware mode, this bit will be kept “1” until OC release; in software mode, this bit will be kept “1” until software clears it by writing “1” into this bit.

Bit1 (UV_DSBL): This bit is set to “1” when the time of UV equals to UV delay. In hardware mode, this bit will be kept “1” until UV release; in software mode, this bit will be kept “1” until software clears it by writing “1” into this bit.

Bit0 (OV_DSBL): This bit is set to “1” when the time of OV equals to OV delay. In hardware mode, this bit will be kept “1” until OV release; in software mode, this bit will be kept “1” until software clears it by writing “1” into this bit.

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Register 20h – Charge/discharge State Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	reserved	reserved	reserved	CHG_ST (R)	DSG_ST (R)	reserved	reserved

Default value is 8’h0. This register indicates the chip is in discharge state or charge state which is detected by comparing the ADC current data with the discharge state threshold or the charge state threshold. Refer to “EEPROM Register 28h” section and “EEPROM Register 29h” section for detail.

Bit3 (CHG_ST): If “1”, OZ890 is in charge state.

Bit2 (DSG_ST): If “0”, OZ890 is in discharge state.

==========

Register 22h/23h – Software Bleeding Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
22h	BLD_CL7	BLD_CL6	BLD_CL5	BLD_CL4	BLD_CL3	BLD_CL2	BLD_CL1	BLD_CL0
23h	TCLK_F1	TCLK_F0	BLD_ENB	BLD_CL12	BLD_CL11	BLD_CL10	BLD_CL9	BLD_CL8

Default value is 8’h0 in register 22h and is 8’hc0 in register 23h. These 2 registers are used to control the cell bleeding in software mode. Refer to “Internal/External Bleeding” section for detail.

TCLK_F1 – TCLK_F0: Specify the external clock frequency when selecting the external clock as working clock as follows:

TCLK_F1 – TCLK_F0	TCLK Clock Frequency
2’b00	512KHz
2’b01	1MHz
2’b10	2MHz
2’b11 (Default)	4MHz

BLD_ENB: In software mode, if “1”, enable the cell bleeding specified by BLD_CL12 – BLD_CL0; if “0”, disable the cell bleeding. In hardware mode, this bit and BLD_CL12 – BLD_CL0 are ignored.

BLD_CL12 – BLD_CL0: Specify the bleeding cells in software mode. If BLD_ENB is “1”, the corresponding cell will be in bleeding if the bit is “1”.

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Register 24h – ADC Request Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_RES1	ADC_RES0	ADC_CH5	ADC_CH4	ADC_CH3	ADC_CH2	ADC_CH1	ADC_CH0

Default value is 8'h0.

Bit7 – Bit6 (ADC_RES1 – ADC_RES0): Specify the ADC resolution for the ADC requested by Microprocessor as follows:

ADC_RES1 – ADC_RES0	ADC Resolution
2'b00	13 bits
2'b01	14 bits
2'b10	15 bits
2'b11	16 bits

Bit5 – Bit0 (ADC_CH5 – ADC_CH0): Specify the ADC channel for the ADC requested by Microprocessor as follows:

ADC_CH5 – ADC_CH0	ADC Channel
6'b000000	No ADC channel is selected
6'b000001	Cell1 voltage
6'b000010	Cell2 voltage
6'b000011	Cell3 voltage
6'b000100	Cell4 voltage
6'b000101	Cell5 voltage
6'b000111	Cell6 voltage
6'b000111	Cell7 voltage
6'b001000	Cell8 voltage
6'b001001	Cell9 voltage
6'b001010	Cell10 voltage
6'b001011	Cell11 voltage
6'b001100	Cell12 voltage
6'b001101	Cell13 voltage
6'b001110	GPIO1 voltage
6'b001111	GPIO2 voltage
6'b010000	GPIO3 voltage
6'b010001	Internal temperature
6'b010010	Current
6'b010011	Group1 offset
6'b010100	Group2 offset
6'b010101	Group3 offset
6'b010110	0v in cell-voltage path
6'b010111	0v in current path
6'b011000	0.6v reference in cell-voltage path
6'b011001	2.1v reference in cell-voltage path
6'b011010	0.6v reference for GPIO path
6'b011011	2.1v reference for GPIO path
6'b011100	VR105 reference for GPIO path
6'b011101	VR12 reference for GPIO path
6'b011110	Vbat12's voltage (NiMH Vbat12)
6'b011111	Vbat8's voltage (NiMH Vbat8)
6'b100000	Vbat4's voltage (NiMH Vbat4)
Others	Reserved

Except the regular current, cell voltages, temperature scan during regular ADC scan cycle, OZ890 still reserves the time slot for the Microprocessor requested ADC channel measurements in Software Mode. Refer to "Time Slot in Different Configuration" section for detail. The Microprocessor can send the request to do the ADC measurement for any channel at specified resolution. The measurement result is stored in Operation Register 26h & 27h.

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Register 25h – ADC Busy Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_RES1 (R)	ADC_RES0 (R)	reserved	reserved	reserved	reserved	reserved	ADC_BUSY (R)

Default value is 8'h0.

Bit7 – Bit6 (ADC_RES1 – ADC_RES0): Specify the ADC data resolution stored in Operation Register 26h. Please refer to "Register 26h/27h – ADC Data Register".

Bit0 (ADC_BUSY): If "1", the ADC requested by Microprocessor is not completed; if "0", the ADC requested by Microprocessor is done.

==========

Register 26h/27h – ADC Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	ADC_D7 (R)	ADC_D6 (R)	ADC_D5 (R)	ADC_D4 (R)	ADC_D3 (R)	ADC_D2 (R)	ADC_D1 (R)	ADC_D0 (R)
27h	ADC_D15 (R)	ADC_D14 (R)	ADC_D13 (R)	ADC_D12 (R)	ADC_D11 (R)	ADC_D10 (R)	ADC_D9 (R)	ADC_D8 (R)

Default value is 8'h0 in 26h and 27h.

ADC_D15 – ADC_D0: Store the ADC data in left-justified format as follows:

ADC_RES1 – ADC_RES0	ADC Data
2'b00	13 bits data are stored in ADC_D15 – ADC_D3
2'b01	14 bits data are stored in ADC_D15 – ADC_D2
2'b10	15 bits data are stored in ADC_D15 – ADC_D1
2'b11	16 bits data are stored in ADC_D15 – ADC_D0

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Register 28h/29h – OT/UT Timer Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
28h	G2_OTUT3 (R)	G2_OTUT2 (R)	G2_OTUT1 (R)	G2_OTUT0 (R)	G1_OTUT3 (R)	G1_OTUT2 (R)	G1_OTUT1 (R)	G1_OTUT0 (R)
29h	IT_OTUT3 (R)	IT_OTUT2 (R)	IT_OTUT1 (R)	IT_OTUT0 (R)	G3_OTUT3 (R)	G3_OTUT2 (R)	G3_OTUT1 (R)	G3_OTUT0 (R)

Default value is 8'h0.

G2_OTUT3 – G2_OTUT0: the timer for the GPIO2's OT/UT event delay or release. Its unit is a temperature scan cycle.

G1_OTUT3 – G1_OTUT0: the timer for the GPIO1's OT/UT event delay or release. Its unit is a temperature scan cycle.

IT_OTUT3 – IT_OTUT0: the timer for the internal's OT/UT event delay or release. Its unit is a temperature scan cycle.

G3_OTUT3 – G3_OTUT0: the timer for the GPIO3's OT/UT event delay or release. Its unit is a temperature scan cycle.

==========

Register 2ah – Event Enable Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCN_EVT_ ENB	ADC_EVT_ ENB	UT_EVT_ ENB	OT_EVT_ ENB	SC_EVT_ ENB	OC_EVT_ ENB	UV_EVT_ ENB	OV_EVT_ ENB

Default value is 8'h0.

Bit7 (SCN_EVT_ENB): If "1", enable scan event to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit6 (ADC_EVT_ENB): If "1", enable ADC event to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit5 (UT_EVT_ENB): If “1”, enable UT event to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit4 (OT_EVT_ENB): If “1”, enable OT event to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit3 (SC_EVT_ENB): If “1”, enable SC event to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit2 (OC_EVT_ENB): If “1”, enable OC event to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit1 (UV_EVT_ENB): If “1”, enable UV event to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit0 (OV_EVT_ENB): If “1”, enable OV event to make the ALERTN pin low active to send an interrupt to Microprocessor.

==========

Register 2bh – Event Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCN_EVT	ADC_EVT	UT_EVT	OT_EVT	SC_EVT	OC_EVT	UV_EVT	OV_EVT

Default value is 8’h0.

Bit7 (SCN_EVT): When an ADC scan is completed, this bit will be set to “1” and be kept “1” until host clears it by writing “1” into this bit.

Bit6 (ADC_EVT): When the requested ADC is completed, this bit will be set to “1” and be kept as “1” until host clear it by writing “1” into this bit.

Bit5 (UT_EVT): Once under temperature event happens, this bit will be set to “1” and be kept as “1” until host clears it by writing “1” into this bit.

Bit4 (OT_EVT): Once over temperature event happens, this bit will be set to “1” and be kept as “1” until host clears it by writing “1” into this bit.

Bit3 (SC_EVT): Once short circuit event happens, this bit will be set to “1” and be kept as “1” until host clears it by writing “1” into this bit.

Bit2(OC_EVT): Once over current event happens, this bit will be set to “1” and be kept as “1” until host clears it by writing “1” into this bit.

Bit1(UV_EVT): Once under voltage event happens, this bit will be set to “1” and be kept as “1” until host clears it by writing “1” into this bit.

Bit0(OV_EVT): Once over voltage event happens, this bit will be set to “1” and be kept as “1” until host clears it by writing “1” into this bit.

==========

Register 2ch – 1S Timer Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	SC_RLS (R)	TM1S5 (R)	TM1S4 (R)	TM1S3 (R)	TM1S2 (R)	TM1S1 (R)	TM1S0 (R)

Default value is 8’h0.

Bit6 (SC_RLS): Short circuit release signal from SCRL pin. In Software Mode, software can use this information to release the MOSFETs after OC/SC event.

Bit5 – Bit0 (TM1S5 – TM1S0): This timer can be used by the software to calculate the gas gauge. If the scan event enable bit is "1", it will increase 1 per second; and it will be cleared to "0" after Microprocessor reads it and restarts to do the incremental operation. If the scan event enable bit is "0", this timer remains zero.

==========

Register 2dh – GPIO Mode Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
G3_MD1	G3_MD0	G3_RES1	G3_RES0	G2_MD1	G2_MD0	G1_MD1	G1_MD0

Default value is 8'h0.

Bit7 – Bit6 (G3_MD1 – G3_MD0): Select GP3 mode in software mode. In hardware mode, these bits are ignored. The mode selection as follows:

G3_MD1 – G3_MD0	GP3 Mode
2'b00	GPIO3 is an analog input and disabled to scan.
2'b01	GPIO3 is a normal analog input and is scanned as temperature channel.
2'b10	GPIO3 is a general purpose digital input/output and disabled to scan.
2'b11	GPIO3 is a normal analog input and is scanned as a special ADC channel. And in this mode, the current channel is disabled to scan. This mode is useful for other current detection device, like Hall Effect device to detect current.

Bit5 – Bit4 (G3_RES1 – G3_RES0): In software mode, these 2 bits select the GP3's ADC resolution when G3_MD1 – G3_MD0 is 2'b11; it doesn't affect the ADC resolution when Microprocessor requests the GP3 ADC. In Hardware Mode, these bits are ignored. The ADC resolution selection as follows:

G3_RES1 – G3_RES0	GP3's ADC Resolution
2'b00	13-bit
2'b01	14-bit
2'b10	15-bit
2'b11	16-bit

Bit3 – Bit2 (G2_MD1 – G2_MD0): Select GP2 mode in software mode. In hardware mode, these bits are ignored. The mode selection as follows:

G2_MD1 – G2_MD0	GP2 Mode
2'b00	GPIO2 is a normal analog input and is disabled to scan.
2'b01	GPIO2 is a normal analog input and is scanned as temperature channel.
2'b10	GPIO2 is a general purpose digital input/output and is disabled to scan.
2'b11	Reserved.

Bit1 – Bit0 (G1_MD1 – G1_MD0): Select GP1 mode in software mode. In hardware mode, these bits are ignored. The mode selection as follows:

G1_MD1 – G1_MD0	GP1 Mode
2'b00	GPIO1 is a normal analog input and is disabled to scan.
2'b01	GPIO1 is a normal analog input and is scanned as temperature channel.
2'b10	GPIO1 is a general purpose digital input/output and is disabled to scan.

2'b11	Reserved.

==========

Register 2eh – GPIO Event & Data Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
G3_EVT	G2_EVT	G1_EVT	G0_EVT	G3_IN (R)	G2_IN (R)	G1_IN (R)	G0_IN (R)

Default value is 8'h0.

Bit7 (G3_EVT): When GPIO3's input data has a change, G3_EVT will be set to "1" and be kept to "1" until software clears it by writing "1" into this bit.

Bit6 (G2_EVT): When GPIO2's input data has a change, G2_EVT will be set to "1" and be kept to "1" until software clears it by writing "1" into this bit.

Bit5 (G1_EVT): When GPIO1's input data has a change, G1_EVT will be set to "1" and be kept to "1" until software clears it by writing "1" into this bit.

Bit4 (G0_EVT): When GPIO0's input data has a change, G0_EVT will be set to "1" and be kept to "1" until software clears it by writing "1" into this bit.

Bit3 (G3_IN): When G3_MD1 – G3_MD0 is 2'b10 (digital input), this bit is the GPIO3 input data; if G3_MD1 – G3_MD0 is not 2'b10, this bit always is "0".

Bit2 (G2_IN): When G2_MD1 – G2_MD0 is 2'b10 (digital input), this bit is the GPIO2 input data; if G2_MD1 – G2MD0 is not 2'b10, this bit always is "0".

Bit1 (G1_IN): When G1_MD1 – G1_MD0 is 2'b10 (digital input), this bit is the GPIO1 input data; if G1_MD1 – G1MD0 is not 2'b10, this bit always is "0".

Bit0 (G0_IN): GPIO0 input data.

==========

Register 2fh – GP Event Enable Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
G3_EVT_ ENB	G2_EVT_ ENB	G1_EVT_ ENB	G0_EVT_ _ENB	reserved	reserved	reserved	reserved

Default value is 8'h0.

Bit7 (G3_EVT_ENB): If "1", enable G3_EVT (GPIO3 event) to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit6 (G2_EVT_ENB): If "1", enable G2_EVT (GPIO2 event) to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit5 (G1_EVT_ENB): If "1", enable G1_EVT (GPIO1 event) to make the ALERTN pin low active to send an interrupt to Microprocessor.

Bit4 (G0_EVT_ENB): If "1", enable G0_EVT (GPIO0 event) to make the ALERTN pin low active to send an interrupt to Microprocessor.

==========

Register 30h – GPIO Enable & Data Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
G3_OUT_ ENB	G2_OUT_ ENB	G1_OUT_ ENB	G0_OUT_ _ENB	G3_OUT	G2_OUT	G1_OUT	G0_OUT

Default value is 8'h0.

Bit7 (G3_OUT_ENB): If "1", enable to output G3_OUT to GPIO3 pin.

Bit6 (G2_OUT_ENB): If "1", enable to output G2_OUT to GPIO2 pin.

Bit5 (G1_OUT_ENB): If "1", enable to output G1_OUT to GPIO1pin.

Bit4 (G0_OUT_ENB): If "1", enable to output G0_OUT to GPIO0 pin.

Bit3 (G3_OUT): GPIO3's output data.

Bit2 (G2_OUT): GPIO2's output data.

Bit1 (G1_OUT): GPIO1's output data.

Bit0 (G0_OUT): GPIO0's output data.

==========

Register 32h ~ 4bh – Cell ADC Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
N	CELLX④_D4 (R)	CELLX_D3 (R)	CELLX_D2 (R)	CELLX_D1 (R)	CELLX_D0 (R)	reserved	reserved	reserved
N+1	CELLX_D12 (R)	CELLX_D11 (R)	CELLX_D10 (R)	CELLX_D9 (R)	CELLX_D8 (R)	CELLX_D7 (R)	CELLX_D6 (R)	CELLX_D5 (R)

These registers store cell1~cell13's ADC data. All the ADC data already are adjusted with the 1st and 2nd offset cancellation.

If BTYP1 – BTYP0 in EEPROM Register 26h is 2'b11 or 2'b11, CELLX_D12 – CELLX_D0 are 13-bit signed value with 1.22mv LSB to store the cell1~cell13's voltage.

If BTYP1 – BTYP0 is 2'b00 or 2'b01, CELL4_D12 – CELL4_D0 is 13-bit signed value with 4.07mv LSB (0.61mv*20/3) to store the Vbat4 voltage; CELL8_D12 – CELL8_D0 is 13-bit signed value with 8.13mv LSB (0.61mv*40/3) to store the Vbat8 voltage; CELL12_D12 – CELL12_D0 is 13-bit signed value with 12.20mv LSB (0.61mv*60/3) to store the Vbat12 voltage.

==========

Register 4ch ~ 4dh – GPIO1 ADC Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4ch	GPIO1_D4 (R)	GPIO1_D3 (R)	GPIO1_D2 (R)	GPIO1_D1 (R)	GPIO1_D0 (R)	reserved	reserved	reserved
4dfh	GPIO1_D12 (R)	GPIO1_D11 (R)	GPIO1_D10 (R)	GPIO1_D9 (R)	GPIO1_D8 (R)	GPIO1_D7 (R)	GPIO1_D6 (R)	GPIO1_D5 (R)

GPIO1_D12 – GPIO1_D0 is 13-bit signed value with 0.61mv LSB to store the GPIO1 ADC data. The data already is adjusted with the 1st and 2nd offsets cancellation.

==========

Register 4eh ~ 4fh – GPIO2 ADC Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4eh	GPIO2_D4 (R)	GPIO2_D3 (R)	GPIO2_D2 (R)	GPIO2_D1 (R)	GPIO2_D0 (R)	reserved	reserved	reserved

④ X is the number in 1~13.

4fh	GPIO2_D12 (R)	GPIO2_D11 (R)	GPIO2_D10 (R)	GPIO2_D9 (R)	GPIO2_D8 (R)	GPIO2_D7 (R)	GPIO2_D6 (R)	GPIO2_D5 (R)

GPIO2_D12 – GPIO2_D0 is 13-bit signed value with 0.61mv LSB to store the GPIO2 ADC data. The data already is adjusted with the 1st and 2nd offsets cancellation.

==========

Register 50h ~ 51h – GPIO3 ADC Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50h	GPIO3_D7 (R)	GPIO3_D6 (R)	GPIO3_D5 (R)	GPIO3_D4 (R)	GPIO3_D3 (R)	GPIO3_D2 (R)	GPIO3_D1 (R)	GPIO3_D0 (R)
51h	GPIO3_D15 (R)	GPIO3_D14 (R)	GPIO3_D13 (R)	GPIO3_D12 (R)	GPIO3_D11 (R)	GPIO3_D10 (R)	GPIO3_D9 (R)	GPIO3_D8 (R)

This register is used to store GPIO3 ADC data. The data already is adjusted with the 1st and 2nd offsets cancellation.

When G3_MD1 – G3_MD0 in Register 2dh is 2'b00 or 2'b01, GPIO3_D15 – GPIO3_D3 is 13-bit signed value with 0.61mv LSB. When G3_MD1 – G3_MD0 is 2'b11, the GPIO3 data as follows,

G3_RES1 – G3_RES0	GPIO3 Data
2'b00	GPIO3_D15 – GPIO3_D3 is 13-bit signed data with 0.61mv LSB
2'b01	GPIO3_D15 – GPIO3_D2 is 14-bit signed data with 0.31mv LSB
2'b10	GPIO3_D15 – GPIO3_D1 is 15-bit signed data with 0.15mv LSB
2'b11	GPIO3_D15 – GPIO3_D0 is 16-bit signed data with 0.076mv LSB

==========

Register 52h/53h – Internal Temperature ADC Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	INT_D4 (R)	INT _D3 (R)	INT _D2 (R)	INT _D1 (R)	INT _D0 (R)	reserved	reserved	reserved
53h	INT _D12 (R)	INT _D11 (R)	INT _D10 (R)	INT _D9 (R)	INT _D8 (R)	INT _D7 (R)	INT _D6 (R)	INT _D5 (R)

INT_D12 – INT_D0 is 13-bit signed value with 0.61mv LSB to store the internal temperature's ADC data which can be used to calculate the internal temperature by software. Refer to "Internal Temperature Sensor" for detail.

==========

Register 54h/55h – Current Sensor ADC Data Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54h	CRRT_D7 (R)	CRRT_D6 (R)	CRRT_D5 (R)	CRRT_D4 (R)	CRRT_D3 (R)	CRRT_D2 (R)	CRRT_D1 (R)	CRRT_D0 (R)
55h	CRRT_D15 (R)	CRRT_D14 (R)	CRRT_D13 (R)	CRRT_D12 (R)	CRRT_D11 (R)	CRRT_D10 (R)	CRRT_D9 (R)	CRRT_D8 (R)

CRRT_D15 – CRRT_D0 is 16-bit signed value with 7.63uV LSB to store the current sensor's ADC data. The data already is adjusted with the 1st and 2nd offsets cancellation.

==========

Register 56h – Group1 Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GRP1_OS7	GRP1_OS6	GRP1_OS5	GRP1_OS4	GRP1_OS3	GRP1_OS2	GRP1_OS1	GRP1_OS0

In hardware mode, this register is Read Only; in software mode, this register is RW (Read/Write).

GRP1_OS7 – GRP1_OS0 is 8-bit signed value with 1.22mv LSB to store the group1 offset which is used as 1st offset of cell1~cell5 voltage.
Offset = N*1.22v=N*1.22mV (N:-128~127)
So the Group1 Offset range can be -156.16mV~154.95mV

In Hardware Mode, OZ890 will do ADC offset calibration (Updating Register 56h ~ 5bh) every 30 minutes. In Software Mode, OZ890 will not do ADC offset calibration automatically, instead, the Microprocessor can request to do the ADC offset measurement by writing the corresponding registers and get the values, then write the offset value into the corresponding register.
==========

Register 57h – Group2 Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GRP2_OS7	GRP2_OS6	GRP2_OS5	GRP2_OS4	GRP2_OS3	GRP2_OS2	GRP2_OS1	GRP2_OS0

In hardware mode, this register is Read Only; in software mode, this register is RW (Read/Write).

GRP2_OS7 – GRP2_OS0 is 8-bit signed value with 1.22mv LSB to store the group2 offset which is used as 1st offset of cell6~cell9 voltage.
Offset = N*1.22v=N*1.22mV (N:-128~127)
So the Group2 Offset range can be -156.16mV~154.95mV

==========

Register 58h – Group3 Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GRP3_OS7	GRP3_OS6	GRP3_OS5	GRP3_OS4	GRP3_OS3	GRP3_OS2	GRP3_OS1	GRP3_OS0

In hardware mode, this register is Read Only; in software mode, this register is RW (Read/Write).

GRP3_OS7 – GRP3_OS0 is 8-bit signed value with 1.22mv LSB to store the group3 offset which is used as 1st offset of cell10~cell13 voltage.
Offset = N*1.22v=N*1.22mV (N:-128~127)
So the Group3 Offset range can be -156.16mV~154.95mV

==========

Register 59h – GPIO Offset Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GP_OS7	GP_OS6	GP_OS5	GP_OS4	GP_OS3	GP_OS2	GP_OS1	GP_OS0

In hardware mode, this register is Read Only; in software mode, this register is RW (Read/Write).

GP_OS7 – GP_OS0 is 8-bit signed value with 0.61mv LSB to store the GPIO offset which is used as 1st offset of GPIO1, GPIO2 and GPIO3 voltage.
Offset = N*1.22v=N*0.61mV (N:-128~127)
So the GPIO Offset range can be -78.08mV~77.47mV

==========

Register 5ah/5bh – Current Offset Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5ah	CRRT_ OST7	CRRT_ OST6	CRRT_ OST5	CRRT_ OST4	CRRT_ OST3	CRRT_ OST2	CRRT_ OST1	CRRT_ OST0
5bh	reserved	reserved	reserved	reserved	CRRT_ OST11	CRRT_ OST10	CRRT_ OST9	CRRT_ OST8

CRRT_OST11 – CRRT_OST0: 12-bit signed value with 7.63uV LSB to store the current offset which is used as 1st offset of current channel.
Offset = N*7.63uV (N:-2048~2047)
So the current offset can be -15.625mV ~ 15.617mV

In hardware mode, this register is Read Only; in software mode, this register is RW (Read/Write).
==========

Register 5ch/5dh – EEPROM Data Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5ch	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
5dh	EE_D15	EE_D14	EE_D13	EE_D12	EE_D11	EE_D10	EE_D9	EE_D8

Default value is 8'h00.

When writing a word into EEPROM, EE_D15 – EE_D0 is used to store the 16-bit writing data; when reading a word from EEPROM, EE_D15 – EE_D0 is used to store the 16-bit reading-back data.

When writing a byte into EEPROM, EE_D7 – EE_D0 is used to store the 8-bit writing data.

==========

Register 5eh – EEPROM Address Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
reserved	EE_ADDR6	EE_ADDR5	EE_ADDR4	EE_ADDR3	EE_ADDR2	EE_ADDR1	EE_ADDR0

Default value is 8'h00.

EE_ADDR6 – EE_ADDR0: Specify EEPROM access address. EE_ADDR6 – EE_ADDR1 is the EEPROM word address for EEPROM word write and word read; EE_ADDR6 – EE_ADDR0 is the EEPROM byte address for EEPROM byte write.

==========

Register 5fh – EEPROM Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EE_BUSY (R)	EE_MD2	EE_MD1	EE_MD0	EE_CODE3	EE_CODE2	EE_CODE1	EE_COD0

Default value is 8'h00.

Bit 7 (EE_BUSY): EEPROM busy flag. If "1", the EEPROM access requested from Microprocessor is not completed and Microprocessor cannot start another EEPROM access until this bit "0". If "0", the EEPROM access is completed.

Bit 6 – Bit4 (EE_MD2 – EE_MD0): Select EEPROM mode. If set to "101", select EEPROM mode; if set to other value, select non-EEPROM mode. Only in EEPROM mode, Microprocessor can access EEPROM. It is noted that in EEPROM, the ADC safety scan is disabled.

Bit3 – Bit0 (EE_CODE3 – EE_COD0): Specify EEPROM access as follows:

EE_CODE3 – E_CODE0	**EEPROM Access**
4'b0000	No access
4'b0010	EEPROM Word Write
4'b0011	EEPROM Block Erase
4'b0101	EEPROM Word Read
4'b1010	EEPROM Mapping (Block Read)
4'b1011	EEPROM Byte Write
Others	Reserved

==========

Register 69h/6ah – Password Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
69h	PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0
6ah	PWD15	PWD14	PWD13	PWD12	PWD11	PWD10	PWD9	PWD8

Default value is 8'h00. These 2 registers are used for password verification. User can enter the password into these 2 registers for verification. Refer to "EEPROM Protected Data Modification Mechanism" section for detail.

==========

Register 6bh/6ch – Authentication Random Number registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6bh	ATH_NM7 (R)	ATH_NM6 (R)	ATH_NM5 (R)	ATH_NM4 (R)	ATH_NM3 (R)	ATH_NM2 (R)	ATH_NM1 (R)	ATH_NM0 (R)
6ch	ATH_NM15 (R)	ATH_NM14 (R)	ATH_NM13 (R)	ATH_NM12 (R)	ATH_NM11 (R)	ATH_NM10 (R)	ATH_NM9 (R)	ATH_NM8 (R)

These 2 registers are read out for authentication data calculation in the authentication process. Refer to "Authentication Function" section for detail.

==========

Register 6dh/6eh – Authentication Data registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6bh	ATH_D7	ATH_D6	ATH_D5	ATH_D4	ATH_D3	ATH_D2	ATH_D1	ATH_D0
6ch	ATH_D15	ATH_D14	ATH_D13	ATH_D12	ATH_D11	ATH_D10	ATH_D9	ATH_D8

These 2 registers are used to load the authentication data. User can enter the authentication data into these two registers in the authentication process.

==========

Register 6fh – Password/Authentication Status registers

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWD_FAIL (R)	PWD_OK (R)	PWD_BUSY (R)	reserved	ATH_DSG_ FAIL (R)	ATH_DSG_ OK (R)	ATH_CHG_ FAIL (R)	ATH_CHG_ OK (R)

Bit 7 (PWD_FAIL): Password verification failure flag. If "1", password verification is failed. If OZ890 detects 8 times worming password, this bit will be set to "1" to block more password verification.

Bit 6 (PWD_OK): Password verification success flag. If "1", password verification is passed.

Bit5 (PWD_BUSY): Password verification busy flag. If "1", password verification is in processing and the host cannot start next password verification.

Bit3 (ATH_DSG_FAIL): Discharge Authentication failure flag. If "1", the discharge authentication is failed.

Bit2 (ATH_DSG_OK): Discharge Authentication success flag. If "1", the discharge authentication is passed.

Bit1 (ATH_CHG_FAIL): Charge Authentication failure flag. If "1", the charge authentication is failed.

Bit0 (ATH_CHG_OK): Charge Authentication success flag. If "1", the charge authentication is passed.

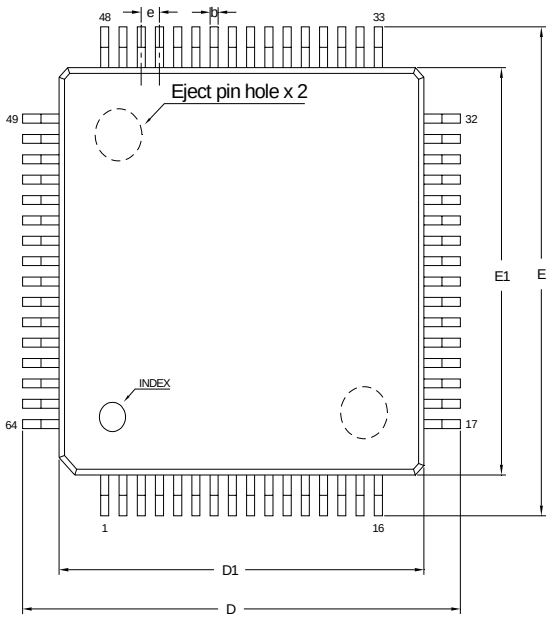
==========

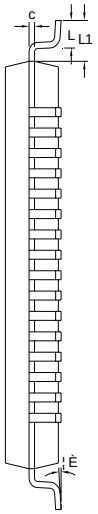
Register 7ch, 7dh, 7fh

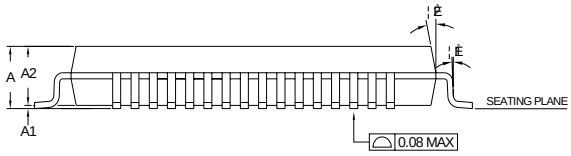
These registers are mapped from EEPROM Register 7ch,7dh, 7fh during EEPROM mapping. When the bit7 "STFRZ" in EEPROM register 7fh is "0", these registers are RW (Read/Write); when the bit7 "STFRZ" in EEPROM register 7fh is "1", these registers cannot be accessed (Not Readable/Not Writable).

PACKAGE INFORMATION

64L LQFP 10x10mm Package Outline Drawing







NOTE:
1. REFER TO JEDEC STD MS-026 BCD
2. Eject Pin hole x 2 (Optional)
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE." DI" AND "E1" ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDE MOLD MISMATCH

SYMBOL	DIMENSION (MM)		
	MIN	NOR	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.50 BSC		
L	0.45	-	0.75
L1	1.00 REF		
θ	0°	-	7°
θ1	0°	-	-
θ2	12° TYP		

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