Low Power Reference Platform

User Guide

Revision History

| Rev.	Date	Author	Description
1	7/07	SJK	Production Release

1. Getting Started

Introduction

It has not been previously feasible to consider FPGA's that are powered by portable battery sources. However reductions in device geometries have significantly reduced static and dynamic power requirements for these devices. The LPRP demonstrates board and chip level, low power design and power management techniques that allow portable, battery operated products to be based on Altera Cyclone III FPGAs .

The LPRP features a Board Level *Power Management Framework (PMF)*. This framework uses techniques to conserve power in the Cyclone III FPGA and at the board level. The PMF is a layer of software run on the Nios II processor in the Cyclone III FPGA and on an additional micro controller.

Five different board Power modes have been defined. They are listed below and will be described in more detail in the Reference Guide. The modes are

Figure 1-1. LPRP Board Power Management Modes

- Normal Mode
- Reduced Mode
- Standby Mode
- Hibernate Mode
- Power Off Mode
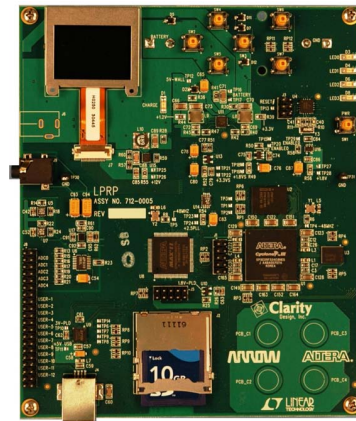
The LPRP is powered by a number of different sources. These include

- A USB Power interface
- A Wall Power supply (DC Power Jack not included)
- Lithium Ion rechargeable batteries

The LPRP can be used to demonstrate low power designs provided with the kit or to develop new ones. It   features the devices listed below.

- EP3C25 Cyclone III Low Cost / Low Power FPGA
- Power Converters form Linear Technology including the LT3455
- CellularRAM, NOR FLASH and removable SD FLASH memory devices
- 1.1 Inch Monochrome Grayscale display
- Audio CODEC and headphone amplifier
- Analog to Digital Converters
- Buttons & LEDS
- General Purpose I/O header
- Ultra low power microcontroller

The LPRP has built in JTAG Debug Hardware that can be used to:

- Download hardware images to the Cyclone III FPGA
- JTAG debug the Nios II processor embedded in the FPGA
- Communicate with the JTAG UART embedded in the FPGA
- Communicate with the SignalTap II Logic Analyzer embedded in the FPGA

This user guide addresses the following topics

- How to install the Development tools
- How to power up and use the LPRP
- How to measure power dissipation
- How to setup and run the example applications

Further Information

For other related information, refer to the following websites:

- For the Cyclone III handbook:
    http://www.altera.com/literature/lit-cyc3.jsp

- For more Cyclone III information:
    http://www.altera.com/products/devices/cyclone3/cy3-index.jsp

- For Cyclone III Orcad symbols:
    http://www.altera.com/support/software/download/pcb/pcb-pcb_in-dex.html

- For Nios® II 32-bit embedded processor solutions:
    http://www.altera.com/technology/embedded/emb-index.html

Software Installation

The instructions in this section describe how to install the following software:

- LPRP Installer
- The Quartus® II Software, Development Kit Web Edition
- Nios II Embedded Development Suite (EDS)

Running the LPRP Installer

The LPRP Installer is located on the 1Gb SD card that is shipped with the kit. It contains the following items:

- The LPRP design examples and board design files
- Quick Start Guide
- LPRP User Guide (this document)
- LPRP Reference Manual

1.Carefully eject the SD card from the LPRP board and plug it into the provided SD card reader. Plug the SD card reader cable into the USB slot on your computer. A Windows Explorer folder should open. Browse to the lprp_setup.exe file and double click on it.

2.Follow the instructions to complete the installation process.

Figure 1-2. LPRP Installed Directory Structure
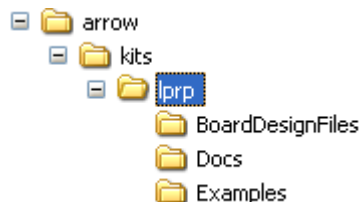
Installing the Altera Development Software

Download and install the following software

- Quartus II Web Edition
- IP Megacore Library
- Nios II Embedded Design Suite

in the order prescribed by performing the following steps:

1. Click on the link to open the Altera download web page
   https://www.altera.com/support/software/download/nios2/dnl-nios2.jsp

2. Download all three software items. Install in the order shown above.

   If you have difficulty installing the Quartus II software, refer to Installing the Quartus II Software in the Quartus II Installation & Licensing Manual for PCs found at www.altera.com.

Licensing the Quartus II Software

Before using the Quartus II software, you must request a license file from the Altera website at www.altera.com/licensing and install it on your PC. When you request a license file, Altera e-mails you a license.dat file that enables the software. To obtain a license, perform the following steps:

3. Go to the Altera website at http://www.altera.com/licensing.
4. Click Quartus II Web Edition Software.
5. Follow the on-line instructions to request your license. A license file is e-mailed to you. Save this file on your computer.
6. Run the Quartus II software.
7. Choose License Setup (Tools menu).
8. Under License File, indicate the license file you received and saved onto your computer in step 5
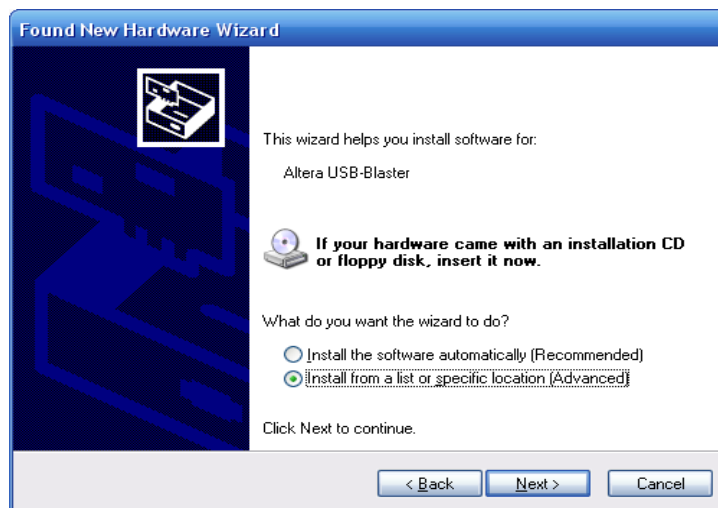
Connecting the LPRP board to a PC

The first time the LPRP board is connected to a PC it will request that appropriate device drivers are installed. Ensure that you have installed the **Quartus II software first** before doing this.
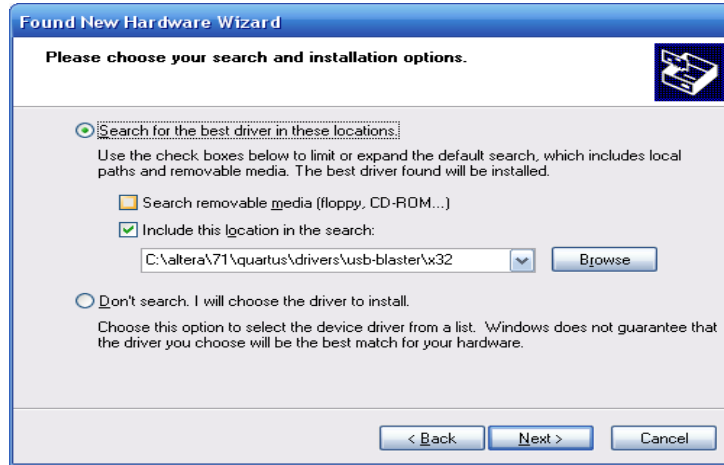
A new hardware wizard will appear. Select "No, not this time and press "Next".

Then select, "Install from a specific location" and press "Next".

Select "Include this location in the search". Browse to the path shown in the picture below and press "Next".

If you see the message shown below, select "Continue Anyway"

Select "Finish" when given the option. Once the driver is installed, the USB host on the PC will negotiate with the USB device on the LPRP. This will allow
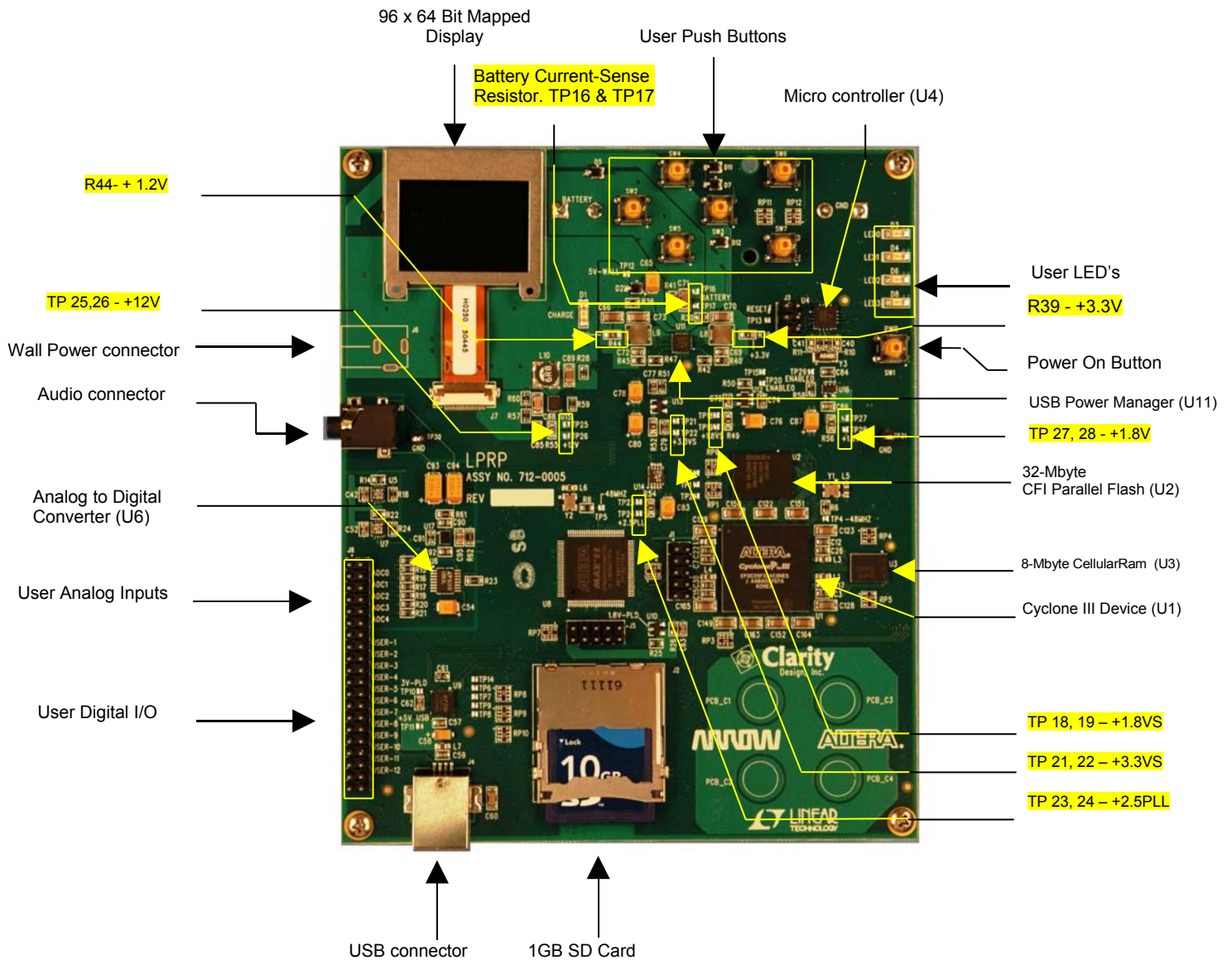
- Full power to be delivered to the board & the Battery can charge
- Quartus will be able to Program the FPGA
- SignalTap II will be able to communicate to any Embedded Logic Analyzers
- Nios II EDS will be able to debug software

2. Using the LPRP Board

LPRP Board Layout

The LPRP is preloaded with a suite of embedded applications. To run these applications and to take advantage of the board features, please familiarize yourself with the board topology shown below. All power measurement points are shown in yellow.

Figure 2-1. LPRP Board Layout

96 x 64 Bit Mapped Display

Battery Current-Sense Resistor. TP16 & TP17

User Push Buttons

Micro controller (U4)

R44- + 1.2V

TP 25,26 - +12V

Wall Power connector

Audio connector

Analog to Digital Converter (U6)

User Analog Inputs

User Digital I/O

User LED's

R39 - +3.3V

Power On Button

USB Power Manager (U11)

TP 27, 28 - +1.8V

32-Mbyte CFI Parallel Flash (U2)

8-Mbyte CellularRam (U3)

Cyclone III Device (U1)

TP 18, 19 – +1.8VS

TP 21, 22 – +3.3VS

TP 23, 24 – +2.5PLL

USB connector

1GB SD Card

Power

Board Power Sources

The PRP is powered from three possible sources.

- A USB Power interface
- A Wall Power supply (DC Power Jack not included)
- Lithium Ion rechargeable batteries

If an external power source (USB or Wall) is used then the Li-Ion Battery is automatically charged. All board power is also drawn from the external power source. If no external power source is available then the board power is drawn from the battery.

Turning Power On

The LPRP board is turned on by pressing the **Power On button**, shown in *Figure 2-1*. When the button is pressed all board functions are turned on. The display turns on and the User Interface (UI) is available for board functional navigation. When the button is pressed again, the board is turned off.

Measuring Power

The LPRP was designed with a focus on power dissipation. It contains a number of different power supplies. The board was designed so that all supplies could be easily measured. For a detailed view of these please see the LPRP Reference Guide. All power measurement test points are highlighted in green in Figure 2-1. The most accurate board measurements can be taken by reading the sense resistor at the battery when external power is *not* applied.

Power Calculation

Power is based on the following calculation $P = V_{supply} * I_{SR}$

where $V_{supply} =$ 1.2, 1.8, 2.5, 3.3, 4.2 or 12 Volts

and $I_{SR} = V_{measured} / R_{SR}$.

The equation can be simplified to $P = V_{measured} * Constant$

Please use Table 1 to assist in deriving power measurements

Table 1. Power Sense Resistors			
Power Supply	**Resistor / Test Point**	**Constant**	**Description**
Battery	R41, TP 16 & 17	$10 * V_{BAT}$	VBAT can vary due to charge level
3.3V	R39	33	Primary Board Supply
1.2V	R44	40	FPGA VCC$_{INT}$
1.8V	R56, TP 27 & 28	18	CellularRam
1.8VS	R49, TP 18 & 19	18	Flash, FPGA VCC$_{IO}$
2.5V	R54, TP 23 & 24	25	FPGA PLL
3.3VS	R52, TP 21 & 22	33	FPGA VCC$_{IO}$, Display, Audio, SD
12V	R55, TP 25 & 26	120	Display

The sense resistor values were chosen so as not to have an intrusive impact on power dissipation. As such, they are very small (all resistors are 0.1Ω except for 1.2V which is .03Ω). When the LPRP board is operating in Normal, Reduced or Standby modes, set the scale on your multimeter to the mV range. When the LPRP board is in Hibernate mode you will need a multimeter that is able to measure values down to 10uV.

The two main board supplies 1.2V & 3.3V are also electronically measured with an on-board analog to digital converter. These values are combined and shown in the display when a track is being played.

The LPRP Reference Manual provides more detail on the power supplies.

3. The User Interface

The LPRP has a very simple menu system as shown below in Figure 3-1. Sub menus can be entered by using the *Up/Down* buttons to navigate and the *Enter* key to select. Press the *Back button* to exit any menu.

The LPRP has two applications. They are the MP3 player and the Photo Viewer. The menu system is described in more detail in the next section.

Figure 3-1. LPRP Menu System
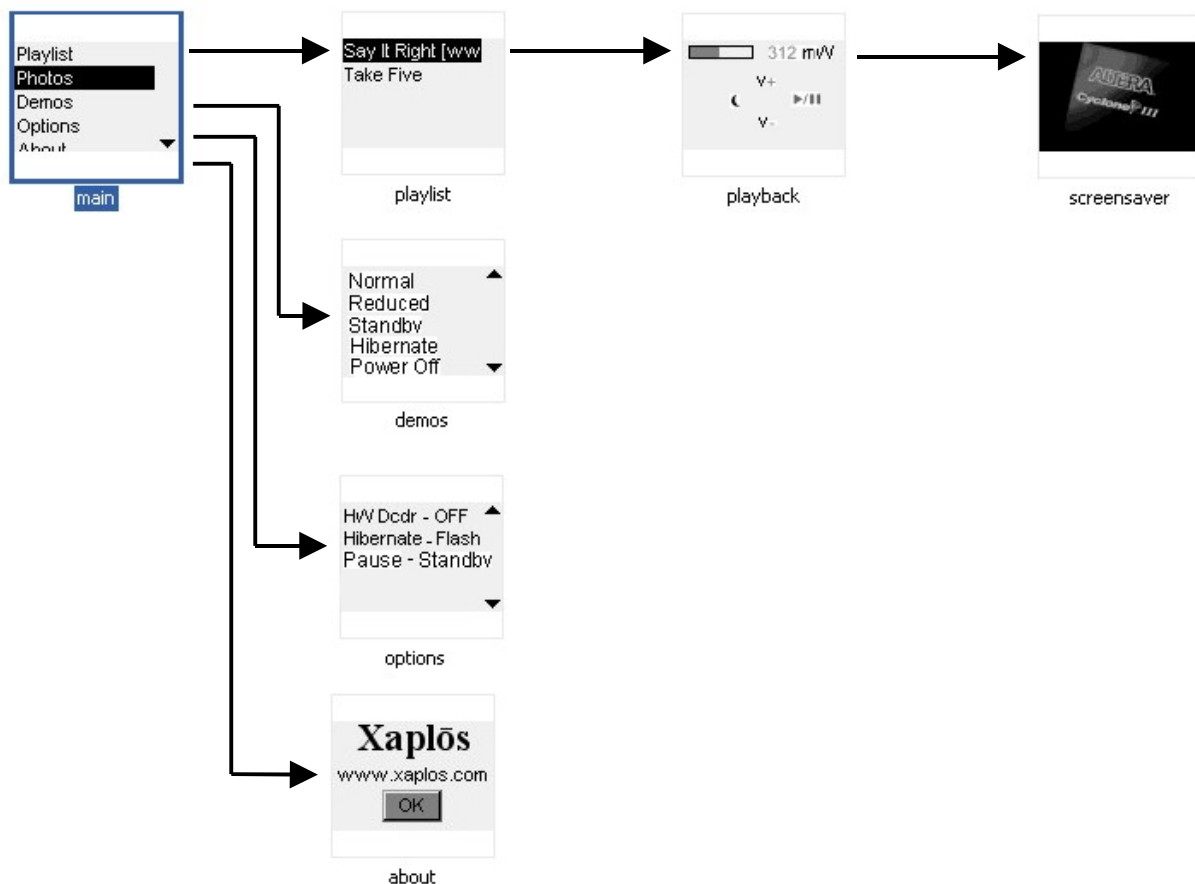
Playlist

A list of available tracks is displayed in the *Playlist* menu. The list is compiled by reading all .mp3 files placed in the /**Music** folder on the SD card. Use the *Up/Down* buttons to navigate and the *Enter* button to start playing. Use the *Back* button to exit.

Playback

The selected track begins to play once the playback menu is displayed. All play options within this menu are selected using the *Left/Right/Up/Down* buttons. The available options are:

Right	- This behaves as a toggle between ***Play*** and ***Pause***
Up/Down	- Volume control
Left	- Hibernates the LPRP. Pressing any key when in Hibernate will restore the LPRP back to its previous mode of operation

Photos

The Photo viewer operates in a slideshow mode. All photos listed in the */Photos* subfolder on the SD card will be displayed. To exit the viewer, press the *Back* button. Photos must be a .bmp format in a 96 x 64 resolution with 16 levels of greyscale. Use a utility such as IrfanView to modify your photos into this format. IrfanView is **only** FREE for home use.

Demos

There are five board level operating modes for the LPRP. The Demo menu allows a user to select a particular mode and then measure the board level power supplies in order to note their effect on power dissipation. Use the *Up/Down* buttons to navigate and the *Enter* button to select. Use the *Back* button to exit a demo mode.

Normal Mode	**-** Audio will begin playing using the Software MP3 decoder
Reduced Mode	**-** Audio will begin playing using the HW accelerator
Standby Mode	**-** All FPGA clocks are halted and the music stops
Hibernate Mode	**-** Context is saved and only the CellularRAM & uC remain on.
Power Off	**-** Only the uC remains on. All board context is lost.

Options

There are three available board options. They all apply to the MP3 player. They are listed below and all operate in a toggle mode. Use the *Up/Down* buttons to navigate and the *Enter* button to toggle. Use the *Back* button to exit.

Hw Dcdr	*- Off:*	MP3 decoder uses software only to decode MP3 tracks
	- On:	MP3 decoder uses HW accelarator to assist in decoding MP3 tracks
Hibernate	*- RAM:*	Hibernate to CellularRAM (Instantaneous)
	- Flash:	Hibernate to Flash (Will take up to 30 seconds)
Pause	*- Normal:*	Audio stops playing. LPRP remains in Normal mode.
	- Standby:	Audio stops playing. LPRP enters Normal mode.

4. Design Examples

Example Designs

The LPRP installer provides a number of hardware and software examples. These are not complete applications but do provide a starting point for future efforts. A list of the examples includes

- hello_fat32   how to use the fat32 file system
- hello_graphics   how to write to the bit mapped display
- hello_pm   how to use the power management framework

A complete Quartus II / SOPC Builder hardware design is also included.

These examples can be found in the Examples sub-directory shown in Figure 1-2.

For a quick introduction to building a Nios II Embedded design in an Altera FPGA and running software on it, please refer to the Nios II Hardware tutorial
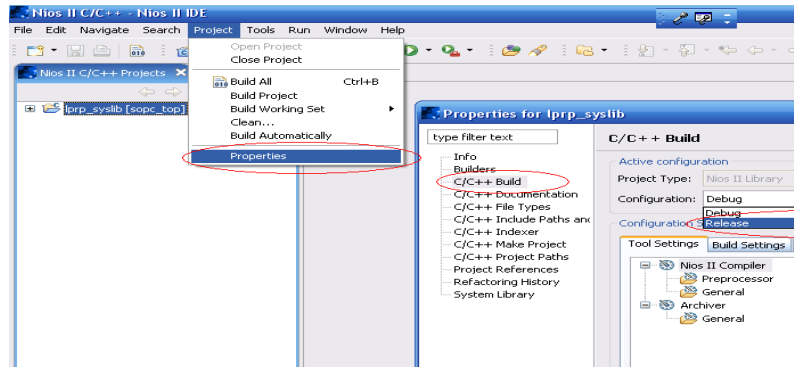
Using the example designs
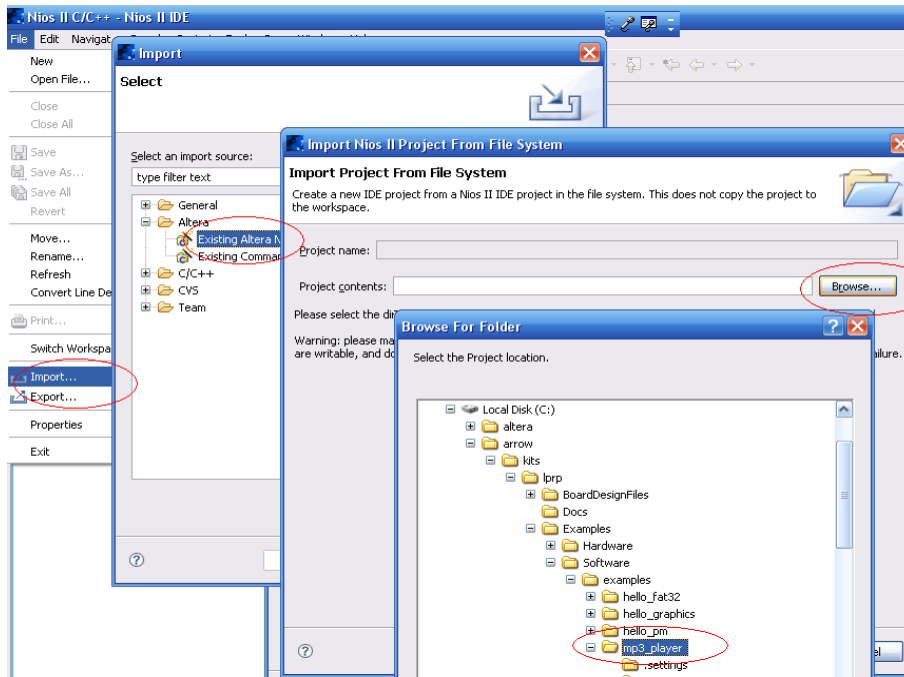
Create a System Library (in the Nios II IDE)
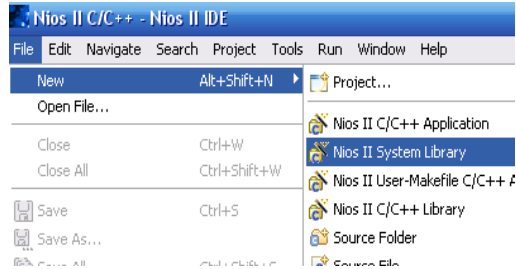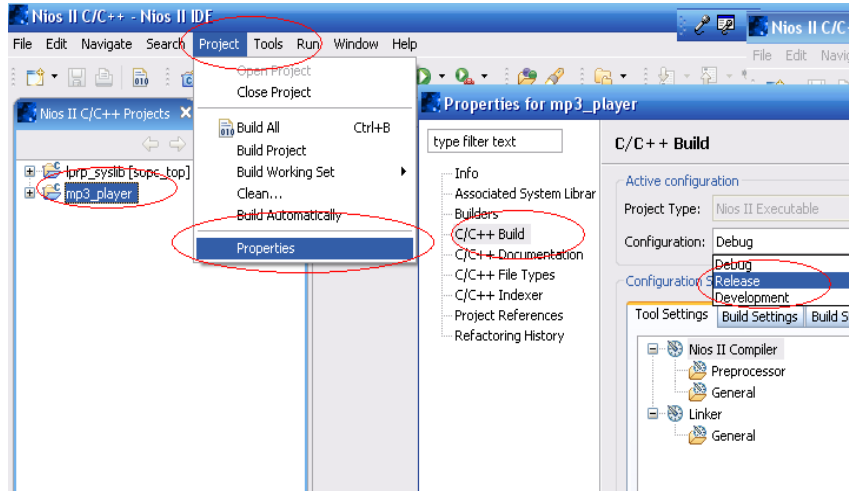

Base it on the correct FPGA hardware design
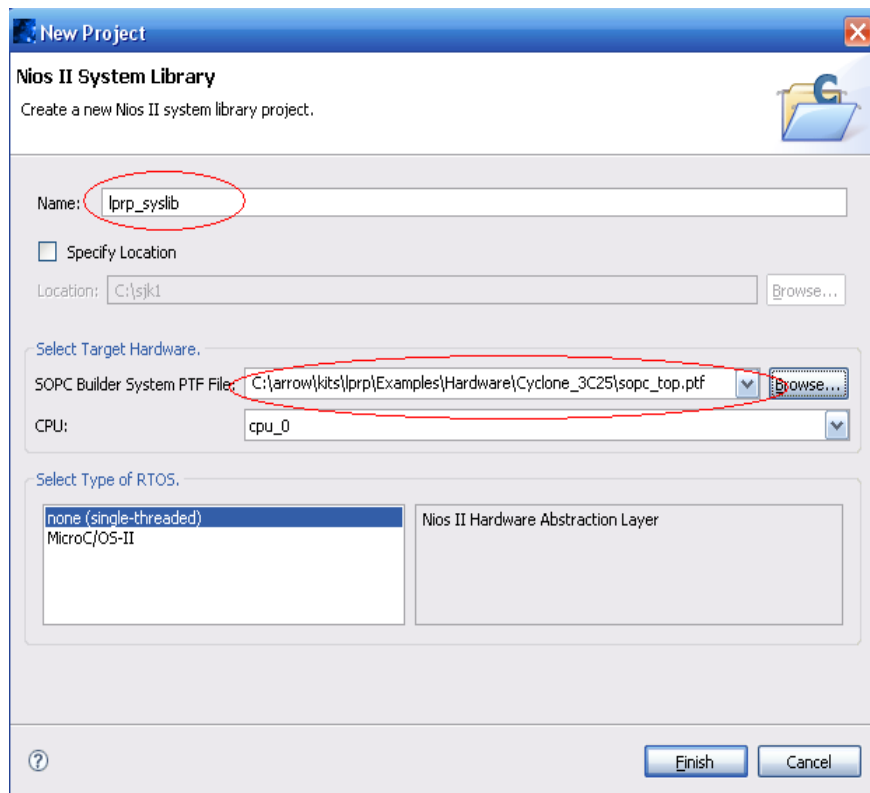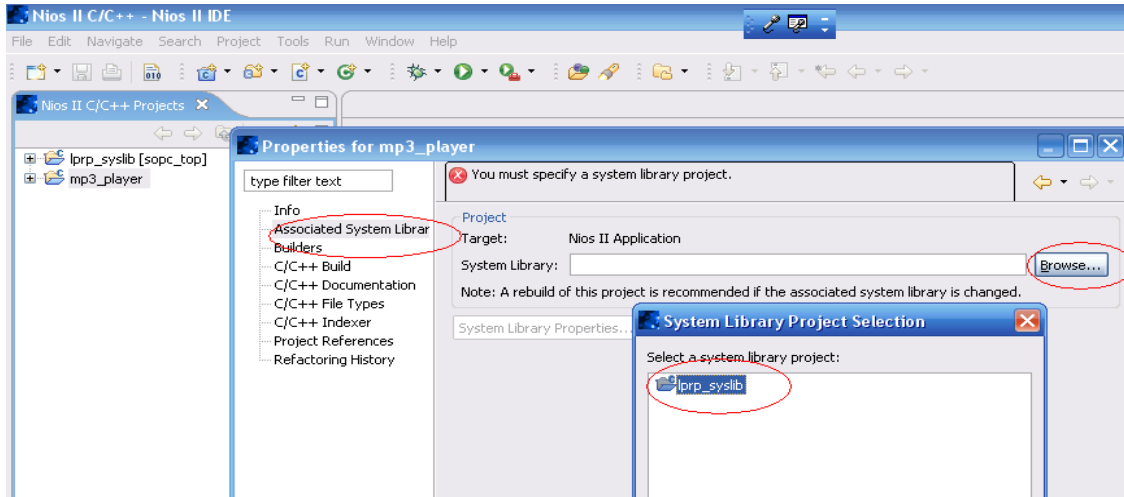
Optimize the Build. Select a Release Build Configuration

Import an Example Project

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Optimize the Build. Select a Release Build Configuration

Associate it with the System Library

Build the project and download it and run it on the LPRP board