Document No. :
Date :

Customer :
Attention :
Your Ref. No. :
Your Part No. :

SPECIFICATIONS

ALPS Model No. : **TSMZ1-603A**
Spec No. :
Sample Status No. : **TSMZ1X601A**

Receipt Status
Approved

By,Date

Signature

Name

Title

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Designed

Approved
Eng. Dept. Communication Devices Division

Sales

Specification of FM Transmitter Module

Rev.2.11

Customer P/N	:	
ALPS P/N	:	TSMZ1-603A
Sample Status	:	TSMZ1X601A

1. Test Conditions
2. General Characteristics
3. Electrical Characteristics
4. Serial Interface
5. RDS data transmission
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7. Test Circuit
8. Referenced Profile for Reflow Soldering
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14. Packing Specifications
15. Reliability Test
16. Handling of this products

This product complies with RoHS Directive.

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1, Test conditions

Usual standard test with next condition, Measurement shall be started 5 minutes after power applied.

The supply voltage must be regulated +3.0V +/-2 %

Condition Temperature : 5 to 35 deg.C

Humidity: 45 to 85 % Rh

If there is an objection to test result, they set up with next test condition.

Condition Temperature : 25+/-2 deg.C

Humidity: 60 to 70 % Rh

2, General Characteristics

2- 1, FM Transmitter General Specifications

Item	Specification
Type	FM Stereo Transmitter with frequency synthesizer
Transmission frequency range	76 - 108.0 MHz
Antenna impedance	nominal 50 Ω
Audio input impedance	100k ohm min.
Operating supply voltage	DC +2.7 V to +3.6 V
Operating Temperature	-30 deg.C to +70degC

2- 2, Mechanical Specifications

Dimensions	See Assembly drawing

3, Electrical Characteristics

3- 1, Absolute Maximum Specification

Item	Symbol	Min.	Max.	Unit
Maximum Supply voltage	VDD	-0.2	3.6	V
Storage temperature	Tstg	-30	80	deg.C

3- 2, Standard Test Condition

Item	Symbol	TEST Condition
Demodulator's audio Filter		Unless designated, Filter used HPF 200Hz / LPF 15kHz
Reference clock frequency		32.768kHz or 19.2MHz (Analog & RDS/RBDS) (X'tal or external clock stability +/- 20ppm max.
Modulation frequency	fi	400Hz
Standard signal level	Vi	140mVrms (ALC OFF)

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3- 3, FM Transmitter Electrical Specification

VDD=3.0+/-0.05V, Ta=25deg.C, f-AF=400Hz, Vi-AF=140mVrms, ALC:OFF, fo:88MHz… otherwise specified.

Item	Symbol	TEST Conditions		Spec. Min.	Spec. Typ.	Spec. Max.	Unit
TX Frequency	fTX			76		108	MHz
Current Consumption	Idd	RFG:0			16	27	mA
Stand by current	Istb					20	uA
TX Output Power	PO	Rl : 50 ohm	RFG : 0	-5.88	-2.88	+0.12	dBm
			RFG : 1		(-0.74)		
			RFG : 2		(+1.36)		
			RFG : 3	+0.30	+3.30	+6.30	
Modulation Deviation	Dev	Pre-emphasis : off		+/- 50	+/- 75	+/- 100	kHz
Modulation Distortion	THD	STEREO Dev : +/- 75kHz				1.5	%
Modulation SN Ratio	SNR	STEREO		48	55		dB
Stereo Separation	SEP	Dev : +/- 75kHz		25	33		dB
Audio Freq. Response	FR	F=50 – 15kHz		-3	0	3	dB
Pilot Tone Level					10		%
RDS Level	RDS				+/-2		kHz

Note: For transmission output level regulations, please adhere to the Radio laws of each country or area.

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4, Serial Interface

This module comprise serial interface mode of the I^2C bus. Data reading and writing are possible with the I^2C bus mode.
The serial interface mode of I^2C bus has two modes in data reading and writing; the bite mode and the multi bite mode.

4- 1, DC Characteristics

Parameter	Symbol	Min	Max	unit
LOW level input voltage (VEX-related input levels)	VIL	-0.5	0.3VEX	V
HIGH level input voltage (VEX-related input levels)	VIH	0.7VEX	VEXmax+0.5	V
Hysteresis of Schmitt trigger inputs: VEX > 2V VEX < 2V	Vhys	 0.05VEX 0.1VEX	 - -	 V V
LOW level output voltage(open drain or open collector) at 3mA sink current: VEX > 2V VEX < 2V	 VOL1 VOL3	 0 0	 0.4 0.2VEX	 V V
Output fall time from VIHmin to VILmax with a bus capacitance of 10pF to 400pF	tof	20+0.1Cb	250	ns
Pulse width of spikes which must be suppressed by the input filter	tSP	0	50	ns
Input current for each I/O pin with an input voltage of 0.1VEX and 0.9VEXmax	Ii	-10	10	μA
Capacitance for each I/O pin	Ci	-	10	pF
Input Low level Voltage Address, DA, CK pins	ViL	-0.4	0.3*VDD	V
Input High level Voltage Address, DA, CK pins	ViH	0.7*VDD	VDD+0.4	V

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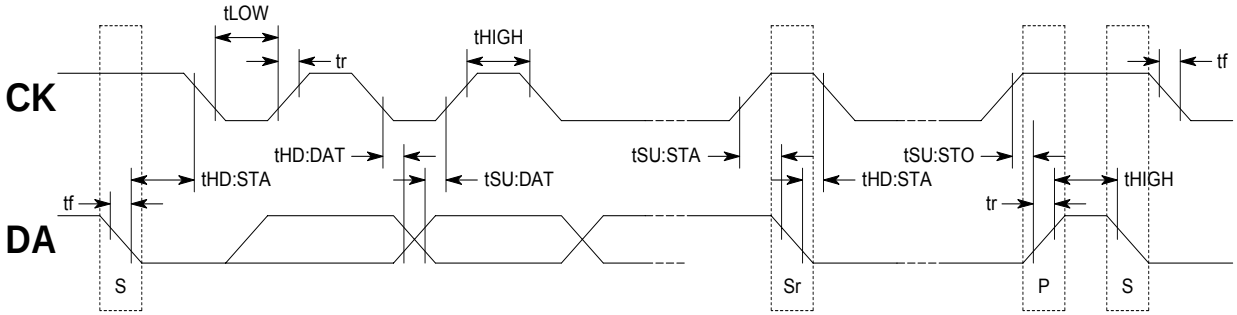
4- 2, I²C Bus Mode

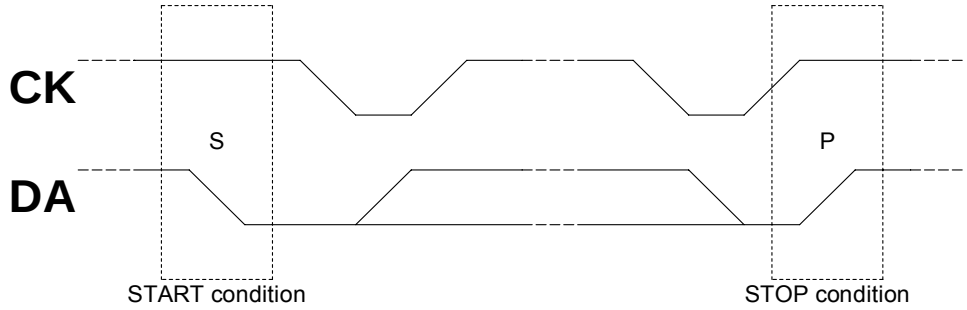
4- 2- 1, AC characteristics



	Symbol	Min	Max	unit
Hold time (repetition START condition)	tHD:STA	0.6	-	µS
Setup time (repetition START condition)	tSU:STA	0.6	-	µS
Data hold time	tHD:DAT	0	0.9	µS
Data setup time	tSU:DAT	100	-	nS
Setup time of STOP condition	tSU:STO	0.6	-	µS
Bus free time of STOP and START conditions		1.3	-	µS
CK clock "L" period	tLOW	1.3	-	µS
CK clock "H" period	tHIGH	0.6	-	µS
Rise time of DA and CK	tr	20+0.1Cb	300	nS
Fall time of DA and CK	tf	20+0.1Cb	300	nS
Bus line capacity	Cb		400	pF

4- 2- 2, Start, Stop Condition

Start condition and Stop condition are respectively required at starting and at ending of the data transfer.



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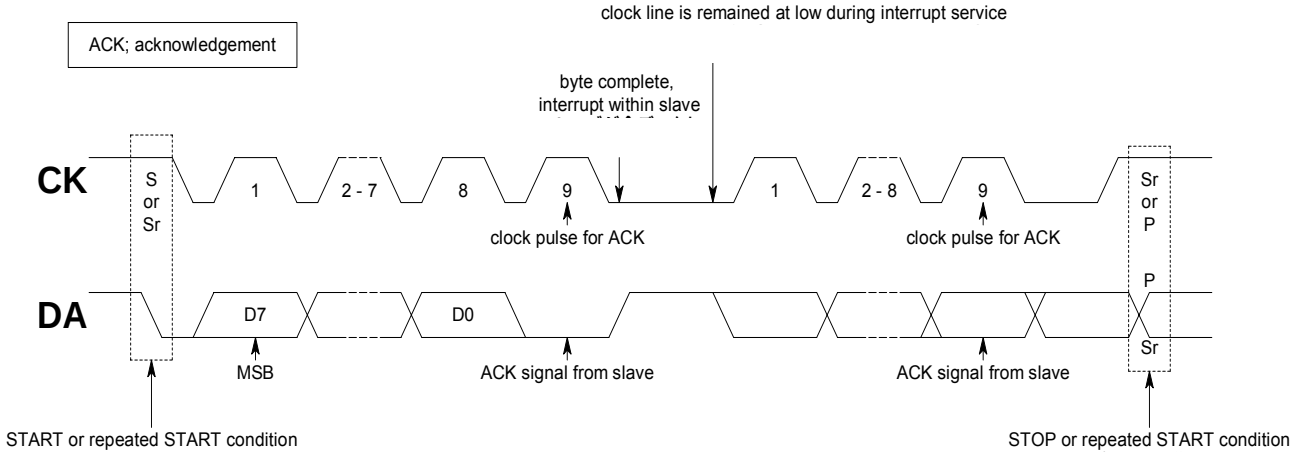
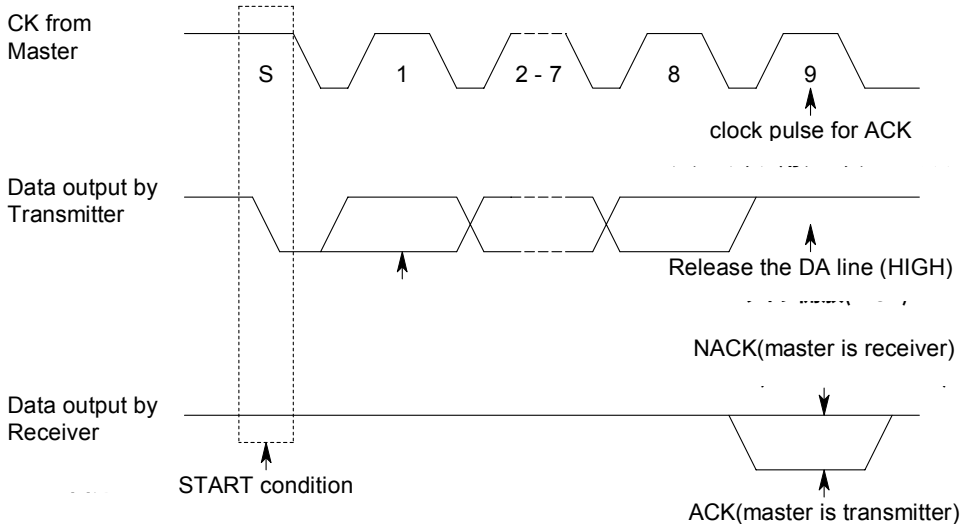
4- 2- 3, Data Transfer

The data length outputted to the DA line is 8 bits. The acknowledge bit is added after the 8 bits data. The data transfer is started with the start condition (Sr) and stopped with the stop condition (P) each generated in the master.



4- 2- 4, Acknowledgement

When the clock pulse for acknowledgement is generated by the master, this module opens the DA line (DA line becomes “H” state). When the acknowledge clock pulse is in the “H” state, this module allows the DA line to be “L” each time it receives 1 bite (8 bits) of data.
When the master operates as a receiver, by not adding the acknowledge bit at the end of data transmitted from the slave, the master informs the ending of the data to this module.



ACK; acknowledgement
NACK; not acknowledgement

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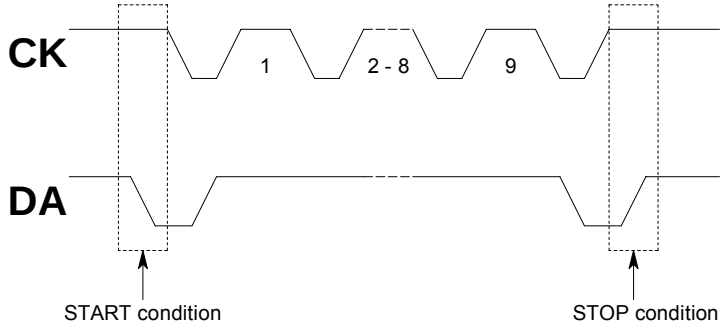
4- 2- 5, Initialization

Perform the following operation to initialize the communication:
Start -> dummy clock ＋ dummy data (1111...) ->stop
Perform the above initialization when an error is occurred during data communication as well.



4- 2- 6, Definition of Bite per One Bite

4-2-6-1, Slave Address

The slave address is composed of the individual address of six bits “110011” and one bit for Address terminal value (AD0). Therefore, Address needs to be HIGH or LOW.
The eighth bit of R/W determines the data direction from the master side.
Data is written when LOW and is read when HIGH.

MSB							LSB
1	1	0	0	1	1	AD0	R/W

4-2-6-2, Resistor address

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

4-2-6-3, Resistor Data

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

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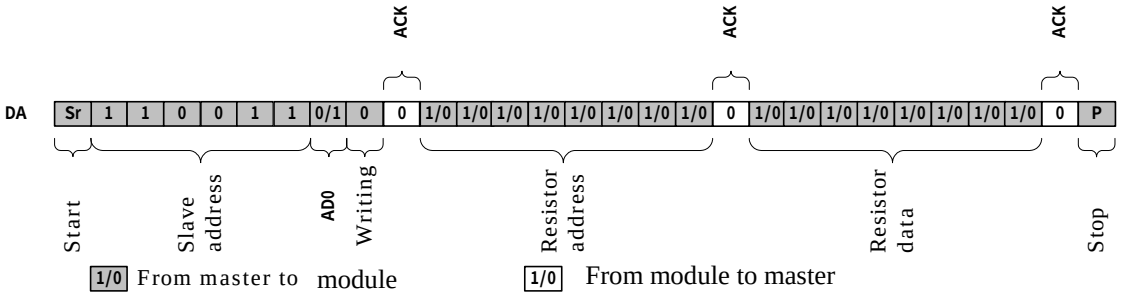
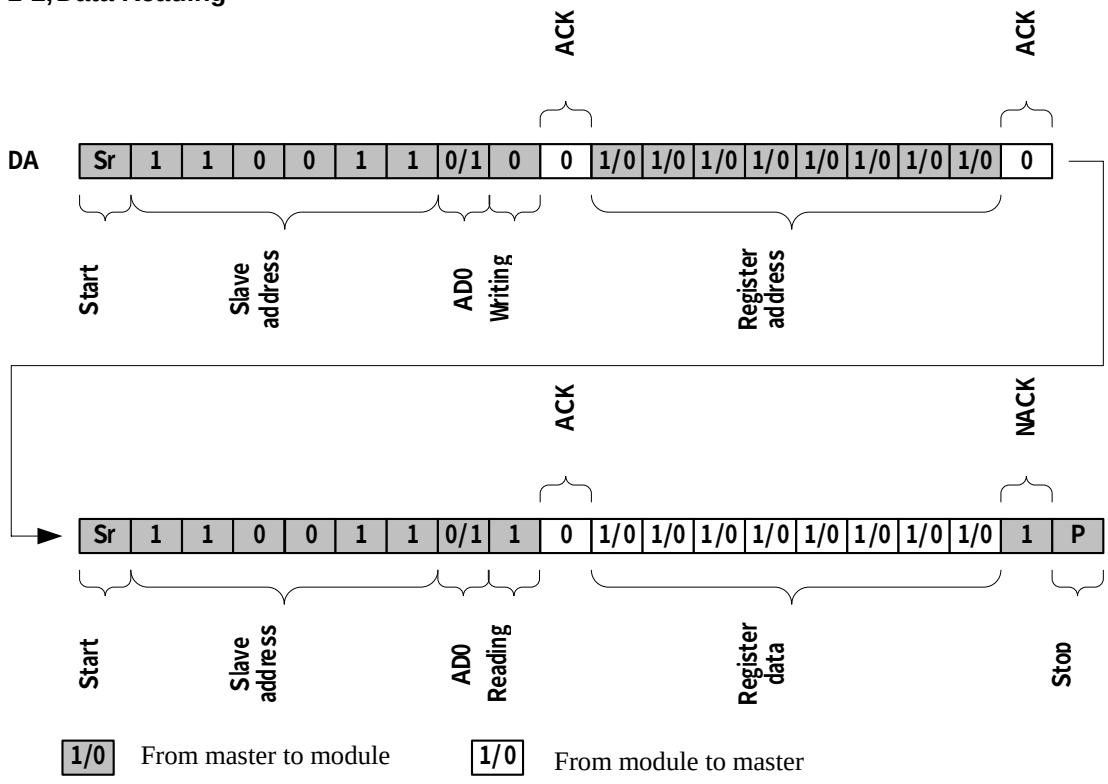
4- 2- 7, Command format

4-2-7-1, Bite Mode

4-2-7-1-1,Data Writing



4-2-7-1-2,Data Reading



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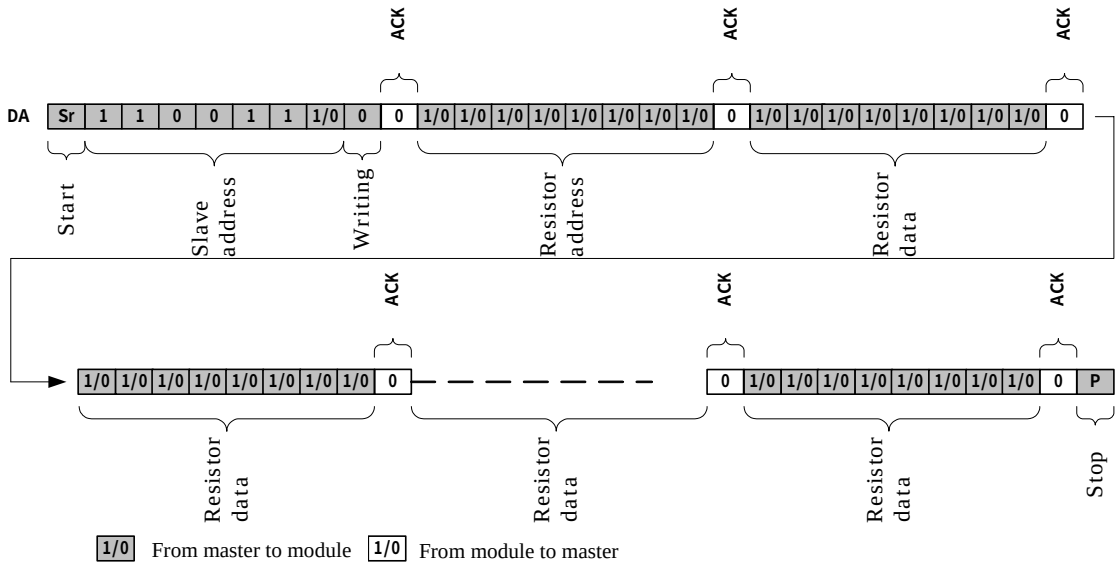
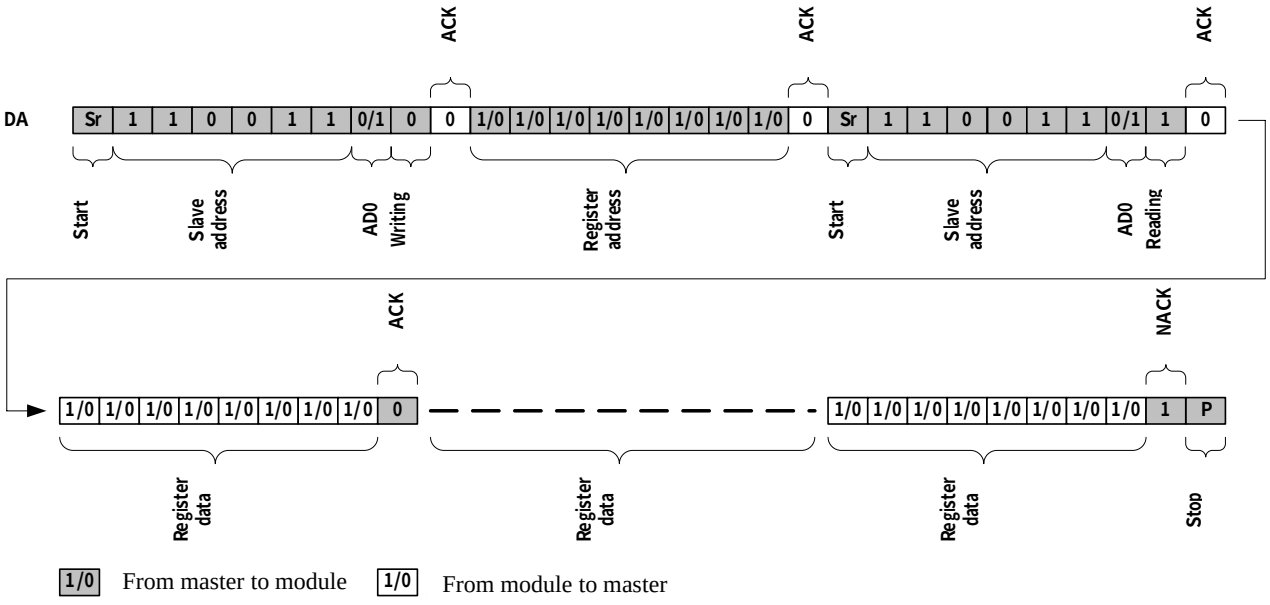
4-2-7-2, Multi Bite Mode

4-2-7-2-1, Data Writing



4-2-7-2-2, Data Reading



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5, RDS Data Transfer

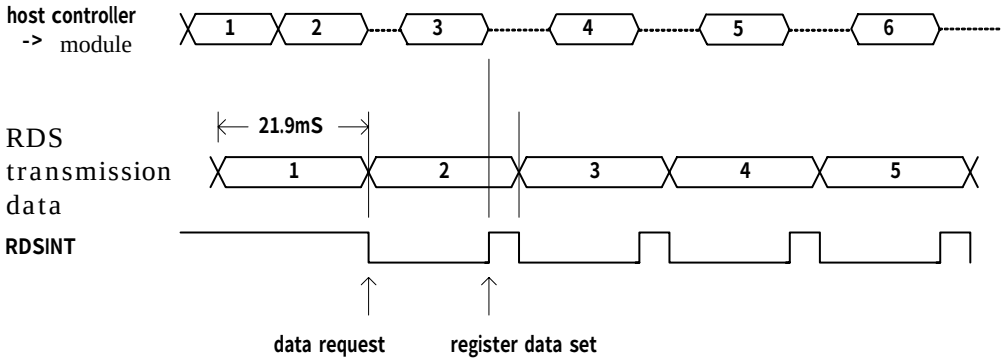
There are two way for RDS data transfer; the 16 bit transmit mode without check word and the 26 bit transmit mode with check word. In either mode, data are transferred in a unit of one block. Mode is alternated by adjusting RDS_CHECKW_CAL resistor.

RDS_CHECKW_CAL＝ 1 -> 16 bite mode

RDS_CHECKW_CAL＝ 0 -> 26 bite mode

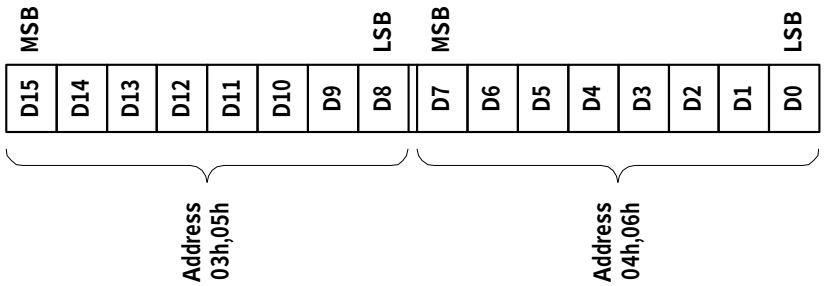
5- 1, RDSINT

As a handshake mean for data communication between Module and the host controller, the RDSINT signal is used. When Module finishes the transmission of the data for one block, the signal is changed from HIGH to LOW. After confirming the period of LOW for RDSINT, transmit the RDS data from the host controller to Module. When the RDS data is placed completely in the resistor of Module, the RDSINT signal is changed from LOW to HIGH. After the RDSINT signal becomes LOW, the host controller needs to transmit the following RDS data to Module within 21.9 mS , the RDS data transition time for one block.
Since Module has the RDS data buffer for two blocks for internal data processing, the host controller can transmit the data for two blocks continuously without checking the LOW signal of RDSINT at starting of the RDS data transmission.



5- 2, Definition of Bite per One Bite

5- 2- 1, 16 Bit Mode



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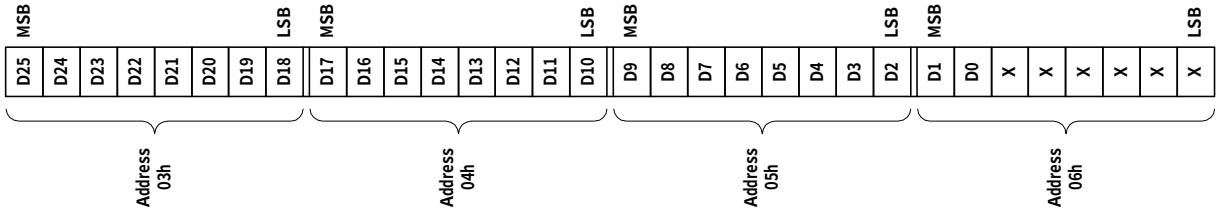
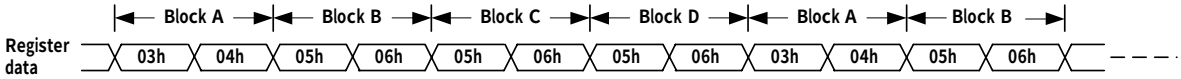
5- 2- 2, 26 Bit Mode



5- 3, Command Format

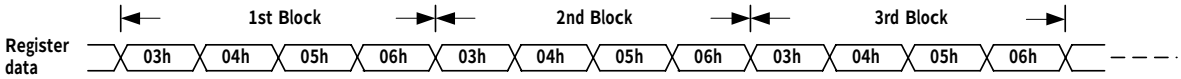
5- 3- 1, 16 Bit Mode

Transmit the data of the first block A with the resistor addresses of 03h and 04h.
Transmit the data of the consecutive blocks B, C and D in sequence each with the resistor addresses of 05h and 06h.
The RDS data block is transmitted from module in the order of A, B, C, and D continuously.



5- 3- 2, 26 Bit Mode

No direction to the order of the block data to be transmitted. The RDS data is transmitted from module according to the order of the data transmitted from the host controller.



6, Software Control Specifications

6- 1, Resister Setting (outline)

After turning IC power ON, set all registers at default values before setting Register PE at “1”.
Refer to the register map for more details. Be sure to set the registers, indicated as gray parts In the register map, at the default values. The registers other than gray parts in the register map can be defined as you like.

6- 2, Reference Clock

1)Use the crystal oscillator with a frequency stability of +/-20ppm of less, if crystal oscillation.
Reference crystal element CL:9pF Co:1.0pF typ. C1:3.4 fF typ. R1:70 kohm max.
2)When the external clock, couple it to the X1(19)pin for clock input using the capacitor and register. Keep the following conditions:
Input level of the clock: MIN=0.4[Vp-p] to MAX=VDD[Vp-p].
Frequency stability:+/-20ppm or less

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6- 3, Resister Map

*) Set the value designated to the gray-colored resisters.

REGISTER	NAME	CONTENTS	SELECTION	DATA (Power on reset)								Default (Hex)
				D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
00h	PE	Power SW	OFF								0	0
			ON								1	
	PEX	Crystal SW	OFF							0		1
			ON							1		
	XSEL	Clock Select	32.768kHz					0	0			0
			19.2MHz					0	1			
	-	-	-				0					0
	XSEL_X	Clock input Select	Crystal, F192			0						0
			X2			1						
	-	-	-	0	0							0
01h	EM	Pre-emphasis switch	OFF								0	1
			ON								1	
	EMS	Pre-emphasis Selection	50μS							0		0
			75μS							1		
	-	-	-					0	0			0
	SUBC	Forced subcarrier	subcarrier ON				0					0
			Subcarrier OFF				1					
	PLT	Pilot tone	OFF	0	0	0						4
			ON	1	0	0						
02h	MUTE	Mute	OFF								0	0
			ON								1	
	-	-	-			0	0	1	0	1		5
	RFG		0	0	0							0
			1	0	1							
			2	1	0							
			3	1	1							

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REGISTER	NAME	CONTENTS	SELECTION	DATA (Power on reset)								Default (Hex)	
				D7	D6	D5	D4	D3	D2	D1	D0		
03h	RDSDATA	RDS data		0	0	0	0	0	0	0	0	0	
04h				0	0	0	0	0	0	0	0		
05h				0	0	0	0	0	0	0	0		
06h				0	0	0	0	0	0	0	0		
07h	P2	Program data for CLK		0	1	1	1	1	1	1	0	Note1	
08h							0	1	1	1	0		
	-	-	-	0	0	0						0	
09h	-	-	-	0	0	0	0	0	0	0	0	08	
0Ah	P	Program data for Synthesizer		0	0	0	0	0	0	0	0	*D3	*Note 2
0Bh				0	0	0	0	0	0	0	0	*23	
0Ch	-	-	-	0	0	0	0	1	1	0	0	0C	
0Dh	ALC_EN	Auto Level Control switch	OFF								0	1	
			ON								1		
	AG	Audio Gain (notALC)	0dB					0	0	0		3	
	ALC_ACTTIMING_SEL	ALC Setting					0					0	
	ALC_CH2_TIMING_SEL	ALC Setting				0						1	
	ALC_TIMEOUT_TIME	ALC Setting		0	0							3	
0Eh	ALC_REC_LVL	ALC Setting						0	0	0	0	0	
	ALC_LOWJUDGE_TIME	ALC Setting				0	0					3	
	-	-	-		0							0	
	ALC_GAINCTRL_SEL	ALC Setting		0								0	
0Fh	ALC_LIM_LVL	ALC Setting						0	0	0	0	0	
	ALC_LIM_PERIOD	ALC Setting				0	0					0	
	SG18	Audio Gain	0dB		0							0	
			-9dB		1								
	RDS_CP	RDS Block Select	Send Block C	0								0	
			Send Block C'	1									

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REGISTER	NAME	CONTENTS	SELECTION	DATA (Power on reset)								Default (Hex)
				D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
10h										0	0	0
	-	-	-					0	0			0
						1	0					2
	RDS_EN	RDS Select	-		0							1
	RDS_CHECKW_ CAL	RDS data format	through	0								0
			with checkword	1								
11h	-	-	-	0	0	0	0	0	1	0	0	E4
12h	-	-	-	0	0	0	0	0	0	0	0	00
13h	-	-	-								0	0
									0	0		1
	-	-	-	0	1	0	0	0				8
14h	-	-	-	0	0	0	0	0	0	0	0	C0
15h	-	-	-						0	0	0.	1
	MAA	Deviation control			1	0	0	0				6
	-	-	-	0								0
16h	-	-	-	1	0	0	0	0	0	0	0	F4
70h	R_CEX	CEX value	(Read only)	*	*	*	*	*	*	*	*	-
7Fh	SRST	for Reset		0	0	0	0	0	0	0	0	Note3

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Note1: In the case of P2 = 3710 (for example), convert decimal to binary.
3710→0 1110 0111 1110 （= 08h[4], ･･･, 08h[0], 07h[7], ･･･, 07h[0]）

REGISTER	NAME	CONTENTS	SELECTION	DATA (Power on reset)								Default (Hex)
				D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
07h	P2			0	1	1	1	1	1	1	0	E7E
08h							0	1	1	1	0	
	-	-	-	0	0	0						0

Note2: In the case of P = 10742 (for example), convert decimal to binary.
10742→0010 1001 1111 0110 （= 0Bh[7], ･･･, 0Bh[0], 0Ah[7], ･･･, 0Ah[0]）

REGISTER	NAME	CONTENTS	SELECTION	DATA (Power on reset)								Default (Hex)
				D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
0Ah	P	Program data for Synthesizer		0	0	0	0	0	0	0	0	29F6
0Bh				0	0	0	0	0	0	0	0	

Note3:Set as “1010 0000” (MSB First) at an appropriate time referring to “8.4. Controller basic operation routines”.

P2 vs. Frequency table:

Please set default value (3710) to the p2 register.

Please do not use the following Frequencies.
S/N deteriorates under influence of a clock beat of the IC inside.

Freq. (MHz)	Freq. (MHz)	Freq. (MHz)	Freq. (MHz)
76.0	85.5	95.0	104.5
77.9	87.4	96.9	106.4
79.8	89.3	98.8	
81.7	91.2	100.7	
83.6	93.1	102.6	

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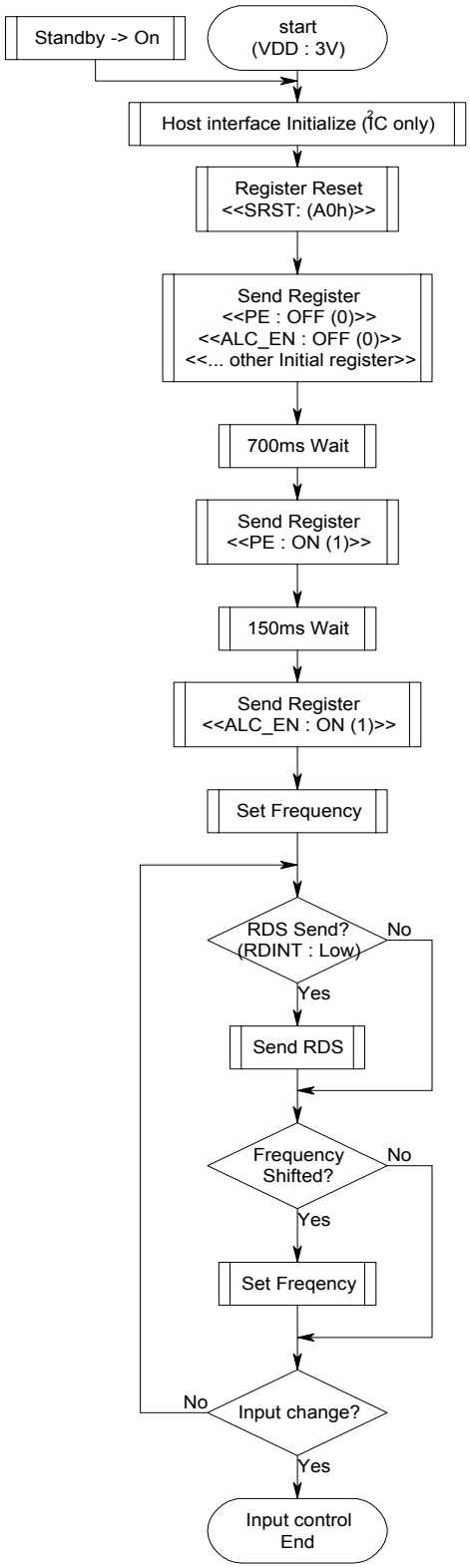
6- 4, Controller basic operation routines



For communication with I^2C, reset the host interface right after the power activation to ensure the communication.

Reset the register.
The register is set to the initial state.

Initial setting while PE=OFF (0).

Wait for about 700ms to stabilize the crystal oscillation.

Then, set PE to ON (1).

Wait for about 150ms.

Set ALC to ON.

When RDINT is low, RDS operates “Send RDS” routine for transmission.

When frequency is changed, operate “Set Frequency” routine for adjustment.

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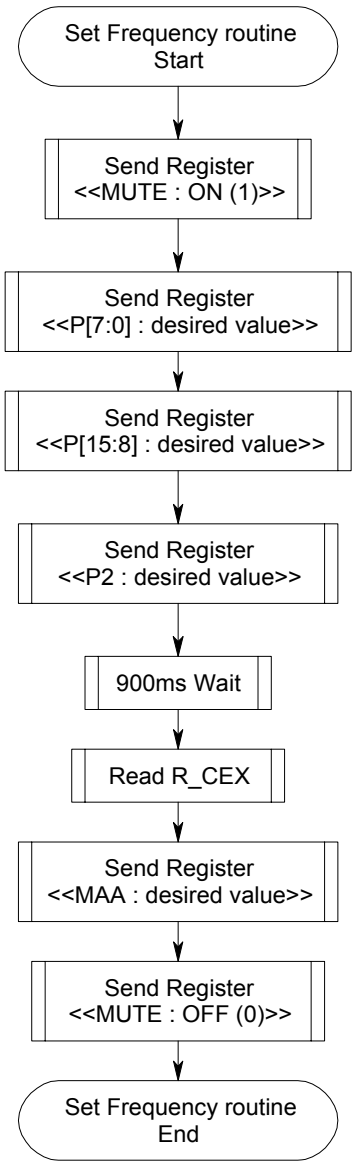

Frequency change flow

Set MUTE to ON (1).

Set a value of P for obtaining desired frequency. Make sure to set a value of address 0Ah first. Right after the 0Bh setting, P value is set.

Based on “P2 vs. frequency” table, set P2 value.

Wait for 900ms for CEX search time.

Read R_CEX.

Based on the correlation table to the CEX, set MAA.

Set MUTE to OFF (0).

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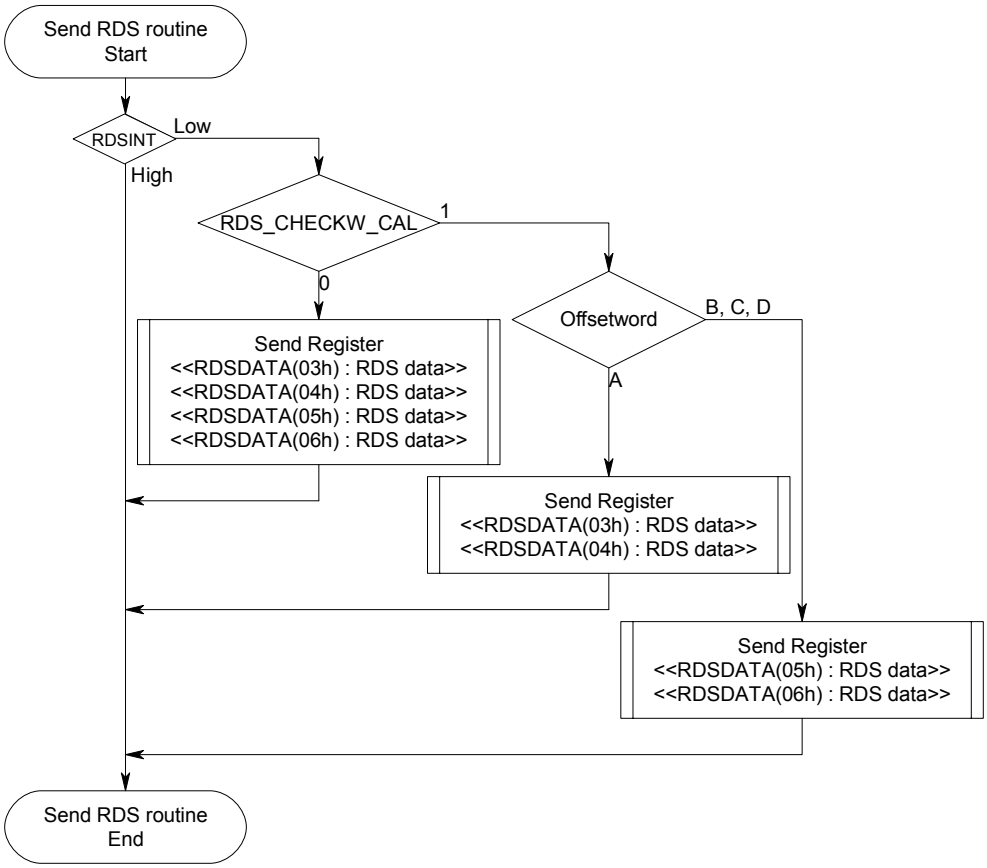

RDS data input flow

Check the status of RDSINT.
When Low, follow the process.
When High, no process.

The process is changed depending on the condition of RDS_CHECKW_CAL.

When RDS_CHECKW_CAL is 0, write the data for 4 Byte of RDSDATA (only 26bit data are effective) regardless of Offsetword.

When RDS_CHECKW_CAL is 1, the area for data writing is changed depending on the Offsetword of data to be transferred.
When Offsetword is A, write the data for 03h and 04h.
When Offsetword is not A, write the data for 05h and 06h.

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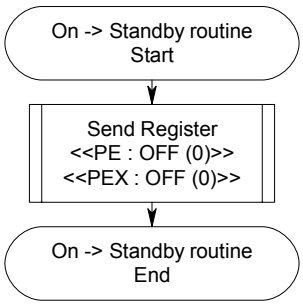
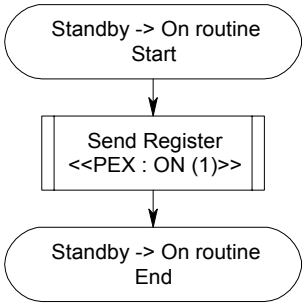


Standby introduction flow

For changing to standby condition, set PE and PEX to OFF (0).



Standby release flow

To release the standby condition, set PEX to ON (1).

6- 5, Resister Specification

6- 5- 1, PE

On or off for power supply is selected.
The power supply for circuits excepting the crystal except oscillation circuit is turned on or off.

0 = Power OFF
1 = Power ON

6- 5- 2, PEX

A crystal oscillator is switched on.
Due to no dependent relationship with Register PE, the crystal oscillation circuit does not stop even when register PE is in "0".

0 = Oscillation circuit stop
1 = Oscillation circuit activate

6- 5- 3, XSEL

A crystal is selected.
An external input reference frequency is selected.
.

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6- 5- 4, XSEL_X

0 = X2 input disable
1 = X2 input enable

6- 5- 5, EM

Presence or absence of pre-emphasis is selected.
0 = Absence of pre-emphasis
1 = Presence of pre-emphasis

6- 5- 6, EMS

The characteristic of pre-emphasis is selected. The presence or absence is depended on Register "EM".
0 = 50μS
1 = 75μS

6- 5- 7, SUBC

The existence of the 38 kHz component containing L-R component of stereo signal is selected. This selection together with the pilot signal setting decides the stereo or monaural of audio signal.
0 = Presence of subcarrier
1 = Absence of subcarrier

6- 5- 8, PLT

A pilot signal ratio is selected. This selection together with the subcarrier setting decides stereo or monaural of audio signal.

PLT[2:0]			Pilot Level
0	0	0	OFF
0	0	1	0.4
0	1	0	0.6
0	1	1	0.8
1	0	0	1.0
1	0	1	1.2
1	1	0	1.4
1	1	1	1.6

6- 5- 9, Mute

During Mute, a sound signal and pilot signal are deleted. Forcibly be monaural and only a carrier is transmitted.
0 = Normal operation
1 = Mute state（Silence condition）

6- 5- 10, RFG

The RF output power is selected.
The output power is adjusted as below by regulating the gains of RF AMP and APC.

RFG[1:0]		Output Power(Typ.)
0	0	0.5mW
0	1	0.8mW
1	0	1.0mW
1	1	2.0mW

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6- 5- 11, RDS Data

Data to be transmitted with RDS are stored. The data to be stored and the data storage area are depending on Register "RDS_CHECKW_CAL"

RDS_CHECKE_CAL		
0	Register03h to Register06h are used for data storage.	
1	Register03h, Register04h:	Data of RDS Block 1
	Register05h, Register06h:	Data of RDS Block 2 to Block 4

6- 5- 12, P2

Program data of 13bit.
VCO oscillation frequency is adjustable.
Adjustable range: “4 (0004h) – 8191 (1FFh)”
Adjustable in Regs 07h and 08h. The adjusted value is reflected as is.
The setting including and rolling forward or backward needs to be carefully adjusted.
For changing from the state of “00FFh” to that of “0100h”, set it up as “01FFh” and then as “00FFh” so as to avoid the state of “0000h”. Or other setting may be applicable.
Obtain the setup value as follows:
Measure S/N between transmission frequencies with 100 kHz step. In the frequency with undesired S/N, decrease the value of P2 by one at the time to find the value which improves S/N. The found value is used as a P2 value for the frequency.
Reference value:
XSEL= 0 or 3: P2[12:0]= 3710 (=0 1110 0111 1110b) (07h[7:0]= 0111 1110, 08h[4:0]= 0 1110)
XSEL= 1 or 2: P2[12:0]= 670 (=0 0010 0101 1111b) (07h[7:0]= 0101 1111, 08h[4:0]= 0 0010)
Minimum value:
XSEL= 0 or 3: P2[12:0] = 3702 (=0 1110 0111 0110b) (07h[7:0]= 0111 0110, 08h[4:0]= 0 1110)
XSEL= 1 or 2: P2[12:0] = 605 (=0 0010 0101 1101b) (07h[7:0]= 0101 1101, 08h[4:0]= 0 0010)

6- 5- 13, P

This is the program data of 16 bit.
The transmission frequency can be changed.
Transmission frequency = reference frequency × *n (*n is an integer.)
Set this value at 256 (P[15:0] = 0b0000 0001 0000 0000) or more.
The value at 255 (P[15:0] = 0b0000 0000 1111 1111) or less is impossible.
The formula for P is shown as below.

$$P = \frac{\text{Transmission frequency}}{\text{Reference frequency (for Frequency calculation)}}$$

The change of Register "0Ah" is reflected when Register "0Bh" is changed. Nothing happens when only the value of Register "0Ah" is changed.
Make sure to change the value of Register "0Bh" after changing the value of Register "0Ah" to reflect the change in Register "0Ah".Control or non-control for output power is decided.
When non-control, a power of 4mW or more is output.
0 = APC OFF（Non control）
1 = APC ON

6- 5- 14, ALC_EN

ALC enable flag
0 = ALC OFF
1 = ALC ON

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6- 5- 15, AG

When ALC_EN=0, the gain value is set by output from CH1/CH2_PGAGAIN.

AG[2:0]			
0	0	0	-9dB
0	0	1	-6dB
0	1	0	-3dB
0	1	1	0dB
1	0	0	+3dB
1	0	1	+6dB
1	1	0	+9dB
1	1	1	?(Don't use)

6- 5- 16, ALC_ACTTIMING_SEL

The timing for gain change during suppressing operation is determined.
0 = Periodical change (depending on "ALC_LIM_PERIOD")
After the input signal exceeds the detection level, the gain is changed in a period of time selected by Register "ALC_LIM_PERIOD". Each gain value of the signal CH1_DATA and the signal CH2_DATA may be the same or different, which depends on the setting of Register "ALC_GAINCTRL_SEL".
1 = Gain change during zero cross (depending on "ALC_TIMEOUT_TIME")
After the input signal exceeds the detection level, the gain is usually changed at the first zero cross. If the zero cross is not generated within the period of time determined by Register "ALC_TIMEOUT_TIME", the gain is changed for the time determined by Register "ALC_TIMEOUT_TIME".
The timing for the gain change of signal CH2_DATA is selected by register"ALC_CH2_TIMINGSEL". Each gain value of the signal CH1_DATA and the signal CH2_DATA may be the same or different, which depends on the setting of Register "ALC_GAINCTRL_SEL".

6- 5- 17, ALC_CH2_TIMING_SEL

The timing for gain change during zero cross is switched.
The timing for gain change to CH2_DATA signal of ALC block is selected.
When Register "ALC_ACTTIMING_SEL" is “0”, the setting in this register is invalid.
0 = Independence
The gain is changed at the time of zero cross of the signal CH2_DATA itself.
1 = Dependence(on CH1_DATA)
The gain is changed at the time of zero cross of the signal CH1_DATA itself.
The zero cross of signal CH2_DATA is ignored.

6- 5- 18, ALC_TIMEOUT_TIME

Zero cross time out
The period for detecting the zero cross, which is the timing for changing the gain in suppression or recovery operation, is determined.
It is “zero cross time out” when the zero cross is not detected during a predetermined period of time.

ALC_TIMEOUT_TIME[1:0]		Detection time	Change cycle(fs = 38kHz)
0	0	384/fs	10ms
0	1	768/fs	20ms
1	0	3072/fs	81ms
1	1	24576/fs	647ms

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6- 5- 19, ALC_REC_LVL

Setting for ALC recovery detection level

ALC_REC_LVL[3:0]				
0	0	0	0	-5dBFS
0	0	0	1	-6dBFS
0	0	1	0	-7dBFS
0	0	1	1	-8dBFS
0	1	0	0	-9dBFS
0	1	0	1	-10dBFS
0	1	1	0	-11dBFS
0	1	1	1	-12dBFS
1	0	0	0	-13dBFS
1	0	0	1	-14dBFS
1	0	1	0	-15dBFS
1	0	1	1	-16dBFS
1	1	0	0	-17dBFS
1	1	0	1	-18dBFS
1	1	1	0	-19dBFS
1	1	1	1	-20dBFS

6- 5- 20, ALC_LOWJUDGE_TIME

Signal detection time for under the recovery level.
The signal which level is less than the recovery detection level for a predetermined period of time shown as below is judged as under the recovery level.

ALC_LOWJUDGE_TIME[1:0]		Detection time	Change period(fs = 38kHz)
0	0	384/fs	10ms
0	1	768/fs	20ms
1	0	3072/fs	81ms
1	1	24576/fs	647ms

6- 5- 21, ALC_GAINCTRL_SEL

The operation with the common ALC gains or with the independent ALC gains in two circuits is selected.
In the case of the operation with the common gains, suppression operation is performed when either CH1 signal or CH2 signal exceeds the suppression level. The recovery operation will continue until either CH1 signal or CH2 signal exceeds the recovery level. The zero detection is referred to CH1.
In the case of the operation with the independent gains, CH1_PGAGAIN and CH2_PGAGAIN are respectively decided according to CH1_DATA signal and CH2_DATA signal.

0 = Gain values are same (common)
1 = Gain values are different (independent)

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6- 5- 22, ALC_LIM_LVL

Setting of ALC suppression detection level

ALC_LIM_LVL[3:0]				
0	0	0	0	-3dBFS
0	0	0	1	-4dBFS
0	0	1	0	-5dBFS
0	0	1	1	-6dBFS
0	1	0	0	-7dBFS
0	1	0	1	-8dBFS
0	1	1	0	-9dBFS
0	1	1	1	-10dBFS
1	0	0	0	-11dBFS
1	0	0	1	-12dBFS
1	0	1	0	-13dBFS
1	0	1	1	-14dBFS
1	1	0	0	-15dBFS
1	1	0	1	-16dBFS
1	1	1	0	-17dBFS
1	1	1	1	-18dBFS

6- 5- 23, ALC_LIM_PERIOD

Gain change period during the suppression. The duration for changing the gain with the suppression is determined. Valid when ALC_ACTTIMING_SEL=0.

ALC_LIM_PERIOD[1:0]		Change period	Change period(fs = 38kHz)
0	0	2/fs	53us
0	1	4/fs	105us
1	0	8/fs	211us
1	1	16/fs	421us

6- 5- 24, SG18

The gain of input audio is adjusted.

0 = 0dB（No adjustment ）
1 = -9dB

6- 5- 25, RDS_CP

In RDS transmission, the offset word of the third block is selected.

0 = C
1 = C'

6- 5- 26, RDS_EN

Transmission or non-transmission of RDS is selected.

0 = non-transmission of RDS
1 = Transmission of RDS

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6- 5- 27, RDS_CHECKW_CAL

Whether check word is attached to the input data or not is selected for data transmission. In RDS data, 26 bit is transmitted as one block. The effective data within the one block is only 16 bit and the other 10 bit is for check word.

<<Regulation for adding check words (especially for Block 2 to Block 4)>>

0 = Through

The data of "Reg03h", "Reg04h", "Reg05h", and "Reg06hBit7 - Reg06hBit6" are transmitted without changed.

1 = Add check word

The check word is attached to the data of "Reg03h" and "Reg04h" in the case of Block1 and is attached to the data of "Reg05h" and "Reg06h" in the case of Block 2 to 4, providing that the check word is in "A" version.

6- 5- 28, MAA

The output level of composite signal is finely adjusted. The adjustment is performed in the analog circuit.

MAA[3:0]				
0	0	0	0	0.428571
0	0	0	1	0.5
0	0	1	0	0.571429
0	0	1	1	0.642857
0	1	0	0	0.714286
0	1	0	1	0.785714
0	1	1	0	0.857143
0	1	1	1	0.928571
1	0	0	0	1
1	0	0	1	1.071429
1	0	1	0	1.142857
1	0	1	1	1.214286
1	1	0	0	1.285714
1	1	0	1	1.357143
1	1	1	0	1.428571
1	1	1	1	1.5

6- 5- 29, R_CEX

＜Read only＞

The status of capacitor in local oscillation circuit is indicated.

When the local oscillation circuit is not controlled automatically, the same value as that of the Register “CEX” is indicated.

On the other hand, when controlled, the status of automatically controlled capacitor in the local oscillation circuit is indicated. In the latter case, the register value has nothing to do with the Register “CEX” value at that time.

6- 5- 30, SRST

Software reset

SRST[7:0]								
1	0	1	0	0	0	0	0	Register initialization

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6 -6 , Setting Items Over the multiple Resistors

6- 6- 1, Reference frequency

6-6-1-1 X1 input (32.768kHz)

PEX (Reg0 Bit1)	XSEL_X (Reg0 Bit5)	XSEL[1:0] (Reg0 Bit3 - 2)	(for Frequency calculation)	Synthesizer Reference Frequency	Local Oscillator Controller Clock	
1	0	0	8.192kHz	32.768kHz	32.768kHz	
		1 - 3	-			-
	1	0 - 3	-			Not use(*3

6-6-1-2 F192 input (19.2MHz)

PEX (Reg0 Bit1)	XSEL_X (Reg0 Bit5)	XSEL[1:0] (Reg0 Bit3 - 2)	(for Frequency calculation)	Synthesizer Reference Frequency	Local Oscillator Controller Clock	
0	0	0	-			Not use(*1
		1	12.5kHz	50kHz	50kHz	-
		2	6.25kHz	25kHz	25kHz	Not use(*2
		3	-			-
	1	0 - 3	-			Not use(*3

6-6-1-3 X2 input (32.768kHz)

PEX (Reg0 Bit1)	XSEL_X (Reg0 Bit5)	XSEL[1:0] (Reg0 Bit3 - 2)	(for Frequency calculation)	Synthesizer Reference Frequency	Local Oscillator Controller Clock	
1	0	0 - 3	-			Not use(*3
	1	0	8.192kHz	32.768kHz	32.768kHz	
		1 - 3	-			-

6-6-1-4 X2 input (19.2MHz)

PEX (Reg0 Bit1)	**XSEL_X (Reg0 Bit5)**	**XSEL[1:0] (Reg0 Bit3 - 2)**	**(for Frequency calculation)**	**Synthesizer Reference Frequency**	**Local Oscillator Controller Clock**	
1	**0**	**0 - 3**	**-**			Not use (***3**
	1	**0**	**-**			Not use (***1**
		1	**12.5kHz**	**50kHz**	**50kHz**	
		2	**6.25kHz**	**25kHz**	**25kHz**	Not use (***2**
		3	**-**			**-**

Note)

*1 : Because of no connection to the terminal to which the reference clock is input, the clock signal does not reach the inside, which result in no operation.

*2 : Caused for abnormal operation in the automatic selection (AUTOCEX) of CEX.

*3 : Control by Register "XSEL_X".

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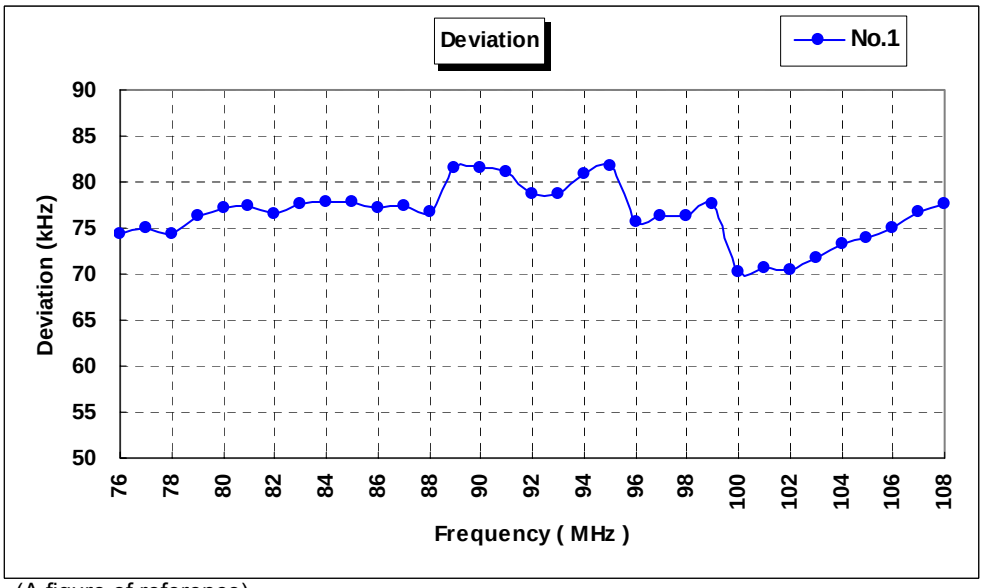
6- 6- 2, Stereo-Monaural Setting

SUBC (Reg1 Bit4)	PLT[2:0] (Reg1 Bit7 - 5)	
1	0	Monaural
0	4	Stereo

6- 7, Setting of Modulation Deviation

Register setting is as follows. Please set "MAA" according to R_CEX.

TX-Freq [MHz]			CEX	MAA
76.0	-	80.0	1	7
75.2	-	83.4	2	6
79.4	-	86.5	3	5
82.6	-	90.5	4	4
86.8	-	92.7	5	4
89.5	-	95.9	6	3
92.4	-	98.1	7	3
94.2	-	100.2	8	2
96.7	-	101.7	9	2
98.2	-	103.5	10	1
100.5	-	104.7	11	1
102.3	-	106.8	12	1
104.3	-	109.1	13	1
106.4	-	111.5	14	0



(A figure of reference)

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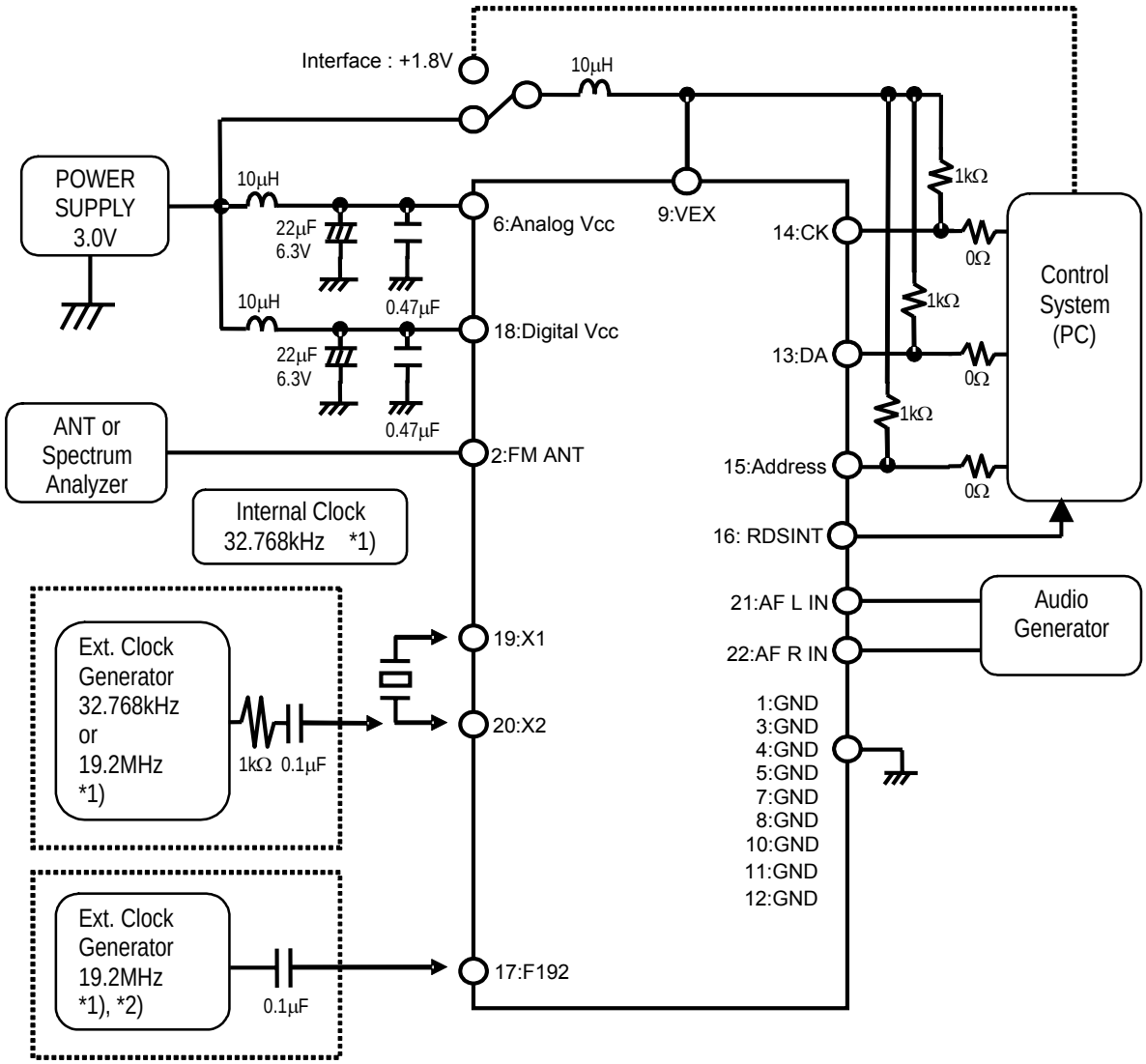
7, Test Circuit

7-1, Test Circuit : Analog Input / RDS and RBDS Transmit



*1)The setting of hope is chosen from among three settings. *2)Please connect it with GND when you do not use it.

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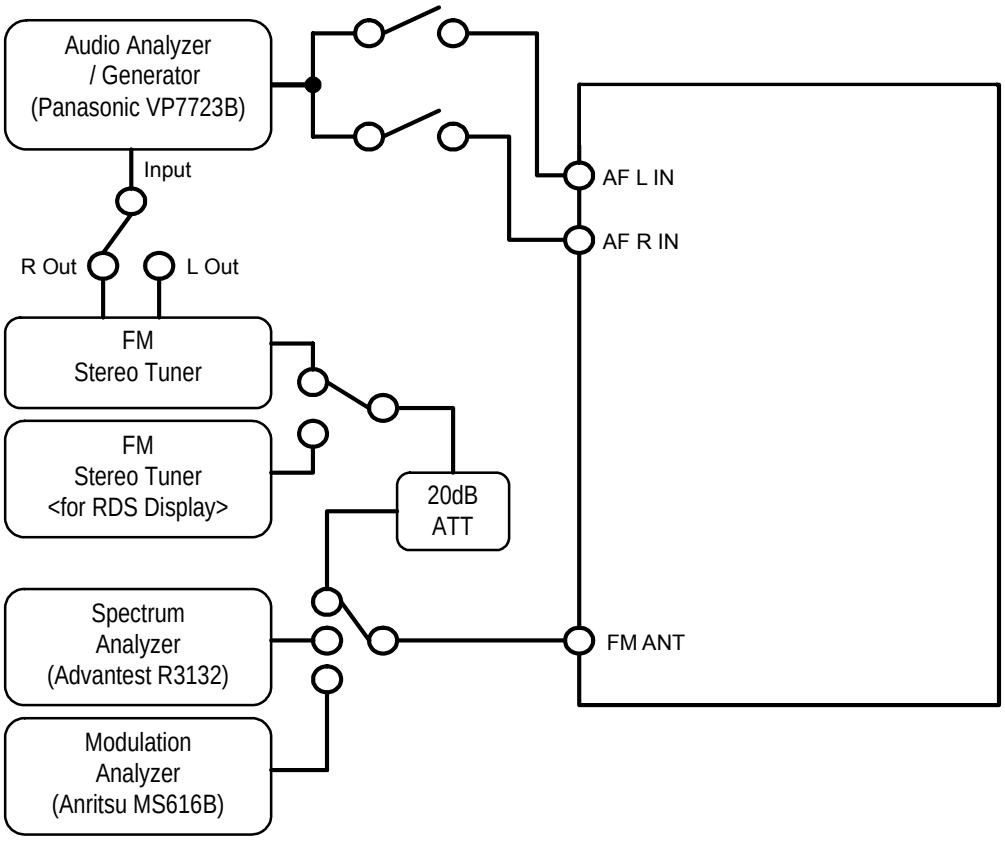
7-2, Measurement Circuit : Analog Input / RDS Transmit.



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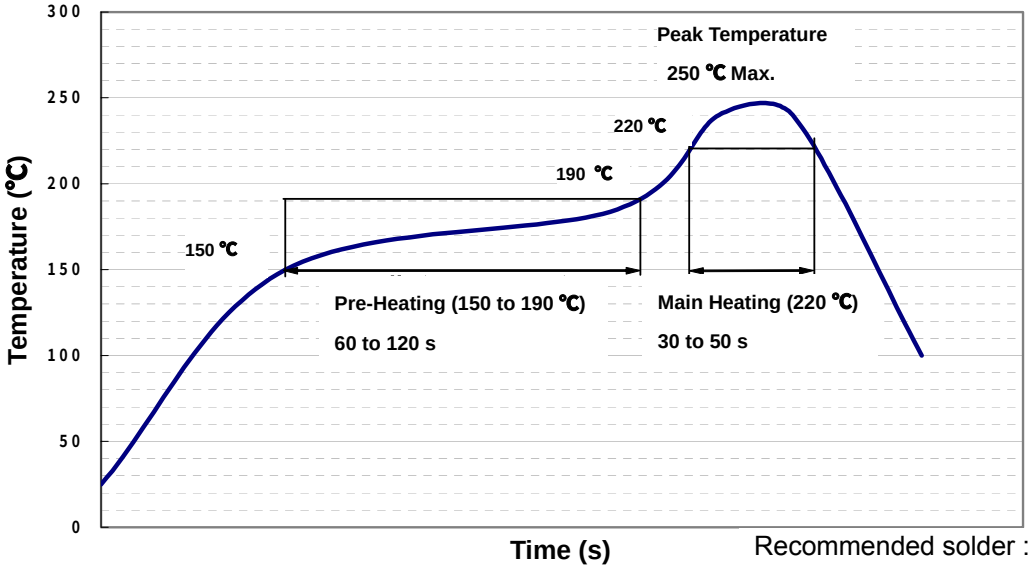
8, Referenced Profile for Reflow Soldering



Recommended solder : Sn-3Ag-0.5Cu

9, Pinning

Pin No.	Pin Name	Description
1	GND	GND
2	FM ANT	RF output
3	GND	GND
4	GND	GND
5	GND	GND
6	ANALOG Vcc	Analog block supply voltage
7	GND	GND
8	GND	GND
9	VEX	MPU power supply
10	GND	GND
11	GND	GND
12	GND	GND
13	DA	Data input/output for Serial interface
14	CK	Clock input for I2C Serial interface
15	ADDRESS	Address set pin Low or High
16	RDSINT	RDS data request output
17*	F192	External reference clock (19.2 MHz) input for IIS
18	DIGITAL Vcc	Digital block supply voltage
19	X 1	X'tal oscillator input 1
20	X 2	X'tal oscillator input 2 / External X'tal oscillator input
21	AF L IN	Audio input left
22	AF R IN	Audio input right

Note : *) Please connect pin 17 with GND when you do not use F192.

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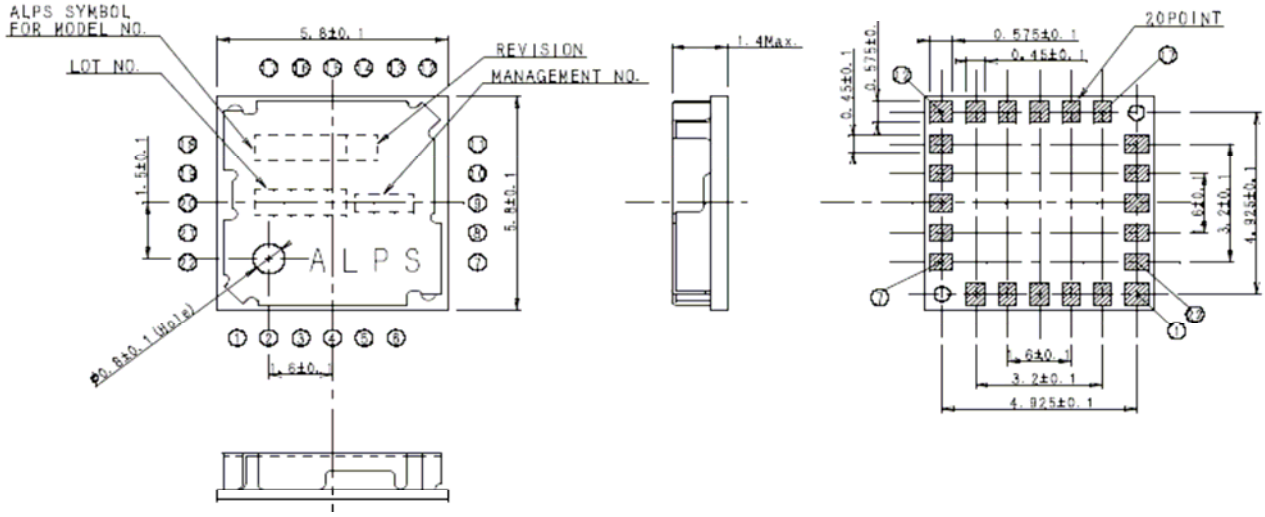
10, Dimension View

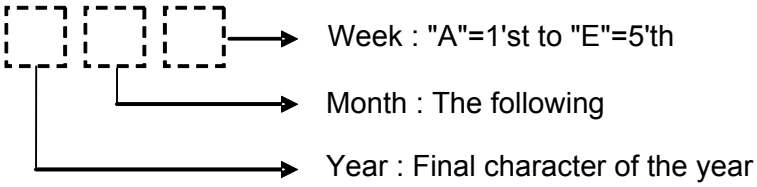


Note

1. We recommend that any signal lines and GND plane should be not laid out under the module.
2. Solderrable surface finishes thickness of nickel and gold flash min. 3 μm / min. 0.05 μm.
3. Coplanarity for soldering pad : 0.1mm max.

ALPS SYMBOL FOR MODEL No.	REVISION
603	A

LOT No. :



Month	1	2	3	4	5	6	7	8	9	10	11	12
Symbol	1	2	3	4	5	6	7	8	9	O	N	D

O : October
N : November
D : December

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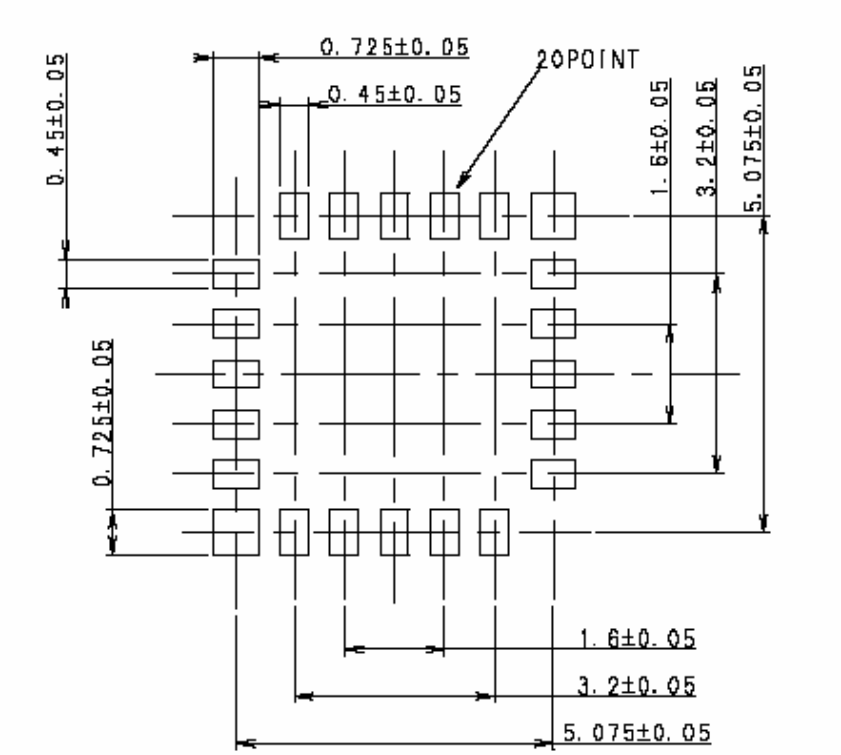
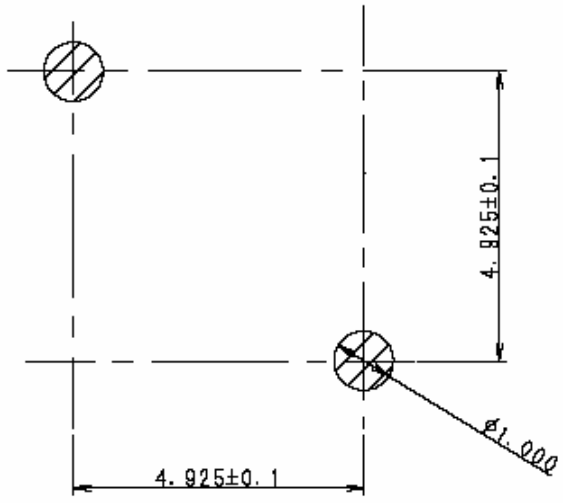
11, Reference for Pads



12, Requirement of Customer's Mother Board Design

Hatching area shall be kept with no copper



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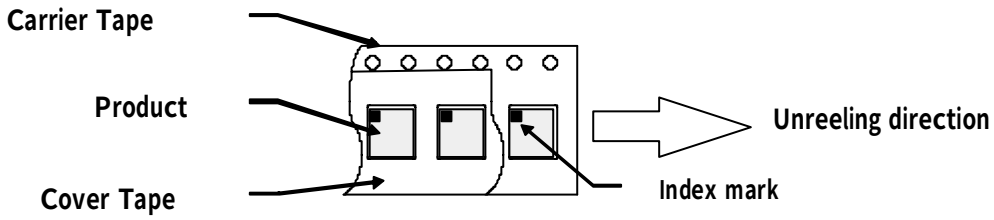
13, Taping Specification

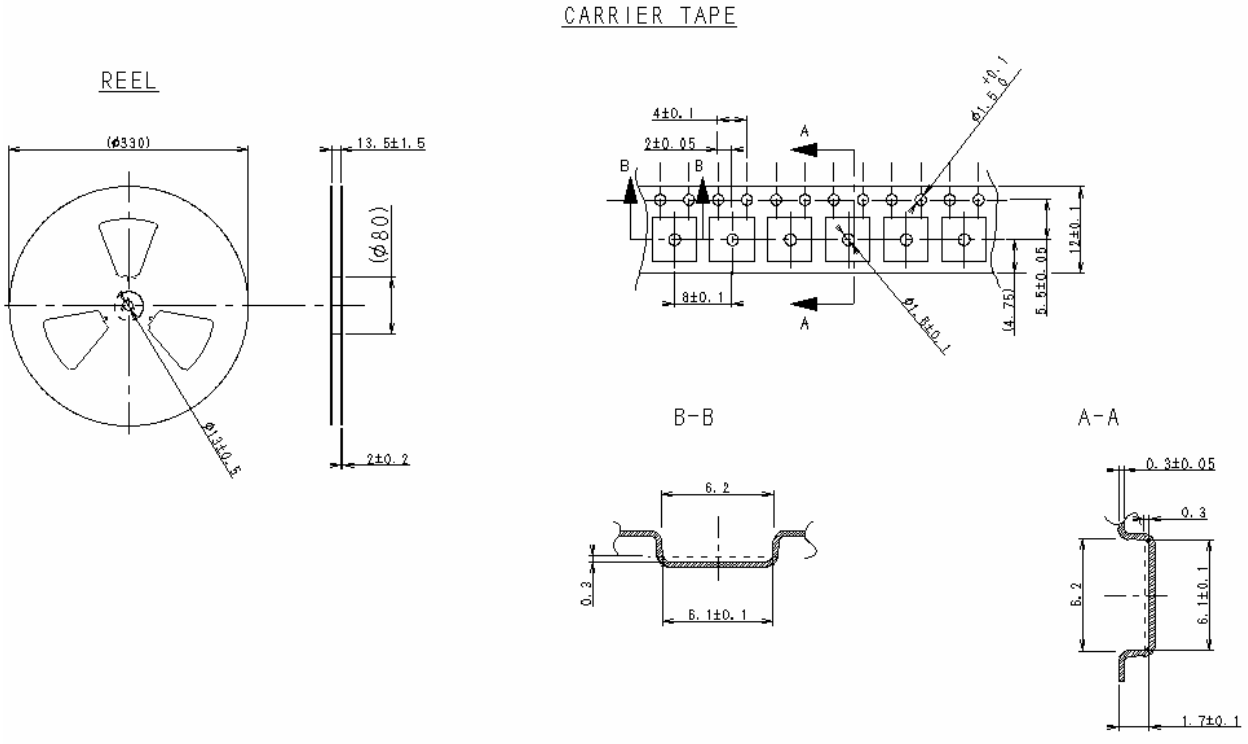
13-1, Materials

Item	Materials
Reel	Conductive Plastics
Carrier Tape	Conductive Plastics
Cover Tape	Conductive Plastics

13-2, Direction of Product



13-3, Dimensions of Carrier Tape and Cover Tape



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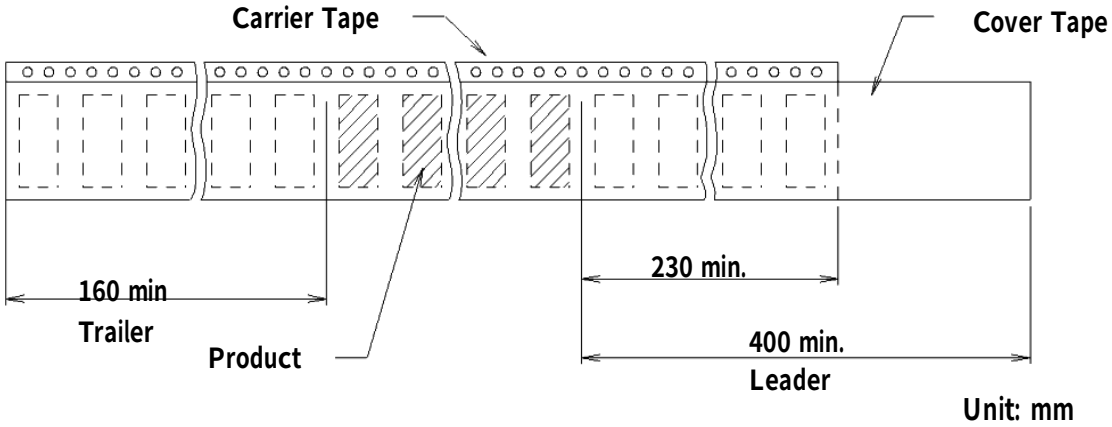
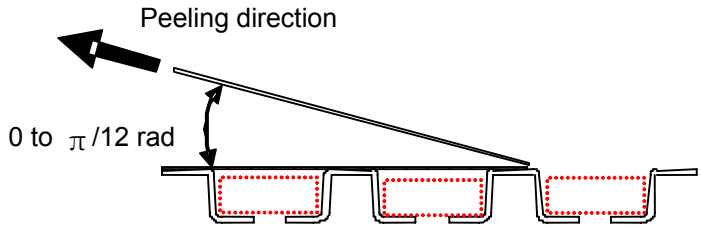
13-4, Leader and Trailer



13-5, Quantity

4,000 pieces / Reel

13-6, Taping Characteristic

Item	Specification
Breaking Force of Cover Tape	0.1 to 1.3 N (Piling Speed : 300 mm / minute) 
Minimum bending radius of Taping	50 mm, 1 time
Falls Characteristic	After the Cover tape peeling, push with 0.1 to 0.2 N. Product falls naturally

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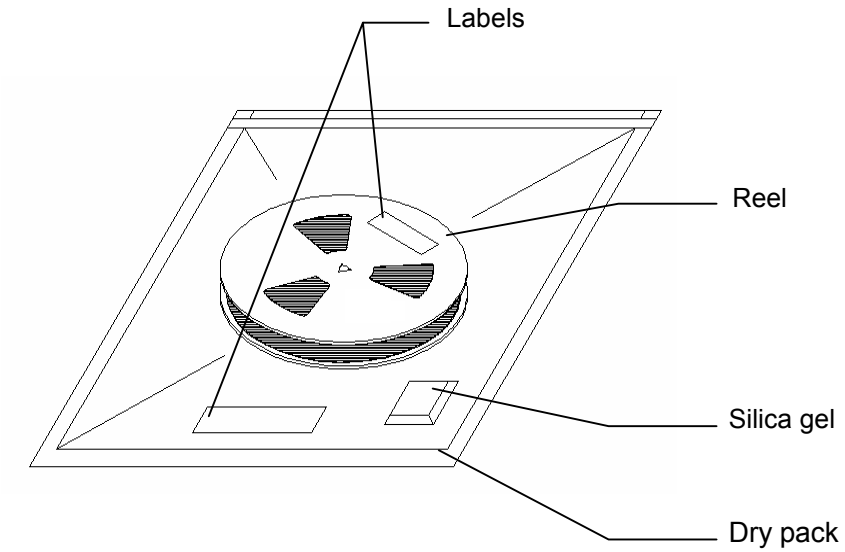
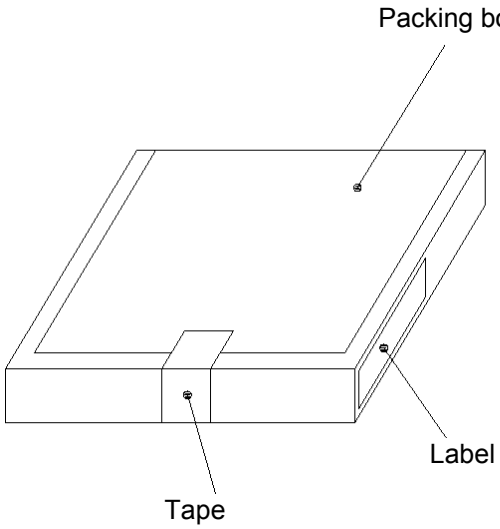
14, Taping Specification

14-1, Dry Pack Condition



14-2, Packing Condition



Note : The Label contents are 14-3.

14-3, Label Marking

Your company name		Quantity	ALPS Model No.		Inspection stamp	
Costomer part No.						

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15, Reliability Test

15-1, High Temperature Test (Non Power Applied)

The sample shall meet the performance of TX Output Power and Stereo Separation.
After storage +60 °C +/- 3 °C for 96 +/- 2 hours.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 2 hours prior to retest.

15-2, Low Temperature Test (Non Power Applied)

The sample shall meet the performance of TX Output Power and Stereo Separation.
After storage -20 °C +/- 3 °C for 96 +/- 2 hours.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 2 hours prior to retest.

15-3, Temperature Cycling Test

The sample shall meet the performance of TX Output Power and Stereo Separation.
After exposed to the temperature -30 °C (30 minutes) to +80 °C (30minutes) for 10 cycles.

15-4, Humidity Test (Non Power Applied)

The sample shall meet the performance of TX Output Power and Stereo Separation.
After storage +40 °C +/- 3 °C and 95 %RH for 96 +/- 2 hours.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 2 hours prior to retest.

15-5, Vibration Test

The sample shall meet the performance of TX Output Power and Stereo Separation after the following.
The sample shall be removed from the test chamber and allowed to stabilize at room ambient conditions for a minimum of 2 hours prior to retest.

Vibration Frequency : 10 to 55 to 10 Hz (1 cycle : 1 minute)
Total Amplitude : 1 mm
Direction : X, Y, Z (each direction 40 minutes)

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15-6, Drop Shock Test

The sample shall meet the performance of TX Output Power and Stereo Separation after the following.

Drop Point (Height) : 1.5 m
Receiving Board : Wood Board (200 mm x 200 mm)
Drop Time : 1 time
Direction : X, Y, Z (each direction)
Mass : 100 g (The module is mounted on the PWB and it put in a plastic case.)

15-7, The Resistance to Reflow Soldering

The sample shall meet the performance of TX Output Power and Stereo Separation. After reflow soldering on the profile.
Based on the following conditions.

15-8, Substrate Bending Test

The sample shall meet the performance of TX Output Power and Stereo Separation. Product should be mounted on Printed Wiring Board.
(Grass Cloth Epoxy Resin, thickness : 1.6mm, W x L : 100 x 40 mm)
When the value of Printed Wiring Board's bowing is 2 mm,
there should be no crack soldering portion.

16, Handling of This Product(Storage Locations of The Product)

(1) Should not contain any noxious gases and the amount of dust should be minimum.
(2) Packing condition
Optimal condition is : 0 to +40 °C, 85 %RH. max.
The storage period is 6 months from the date of the inspection stamp.
(3) After bag is opened
Optimal condition is : 5 to +30 °C, 60 %RH. max.
Devices that will be subjected to reflow solder or other high temperature process must mounted within 168 hours.
(4) Nozzle pressure for module must be a 1N to 3N static load .

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