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| **All Implementation Messages** | **Thu Nov 16 18:19:55 2017** |

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| Program |  | All Implementation Messages - Errors, Warnings, and Infos | New |
| xst | WARNING | HDLCompiler:1127 - "D:\shyamala\IPRC\_isro\unit\_level\_board\_ver\synthesized\_issues\adc\_top\_only\RTL\adc\_top\_interface\_2.v" Line 212: Assignment to en\_sig ignored, since the identifier is never used |  |
| xst | WARNING | HDLCompiler:634 - "D:\shyamala\IPRC\_isro\unit\_level\_board\_ver\synthesized\_issues\adc\_top\_only\RTL\adc\_top\_interface\_2.v" Line 95: Net <data\_in\_from\_bidir[15]> does not have a driver. |  |
| xst | WARNING | Xst:653 - Signal <data\_in\_from\_bidir> is used but never assigned. This sourceless signal will be automatically connected to value GND. |  |
| xst | WARNING | Xst:2677 - Node <adc\_reg\_data\_8> of sequential type is unconnected in block <adc\_top\_interface\_2>. |  |
| xst | WARNING | Xst:2677 - Node <adc\_reg\_data\_9> of sequential type is unconnected in block <adc\_top\_interface\_2>. |  |
| xst | WARNING | Xst:2677 - Node <adc\_reg\_data\_12> of sequential type is unconnected in block <adc\_top\_interface\_2>. |  |
| xst | WARNING | Xst:2677 - Node <adc\_reg\_data\_13> of sequential type is unconnected in block <adc\_top\_interface\_2>. |  |
| xst | WARNING | Xst:2677 - Node <adc\_reg\_data\_8> of sequential type is unconnected in block <adc\_top\_interface\_2>. |  |
| xst | WARNING | Xst:2677 - Node <adc\_reg\_data\_9> of sequential type is unconnected in block <adc\_top\_interface\_2>. |  |
| xst | WARNING | Xst:2677 - Node <adc\_reg\_data\_12> of sequential type is unconnected in block <adc\_top\_interface\_2>. |  |
| xst | WARNING | Xst:2677 - Node <adc\_reg\_data\_13> of sequential type is unconnected in block <adc\_top\_interface\_2>. |  |
| xst | WARNING | Xst:1710 - FF/Latch <regi\_wr\_cntr\_3> (without init value) has a constant value of 0 in block <adc\_top\_interface\_2>. This FF/Latch will be trimmed during the optimization process. |  |
| xst | INFO | Xst:3218 - HDL ADVISOR - The RAM <Mram\_registers\_data> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines. |  |
| xst | INFO | Xst:2261 - The FF/Latch <adc\_reg\_data\_4> in Unit <adc\_top\_interface\_2> is equivalent to the following FF/Latch, which will be removed : <adc\_reg\_data\_5> |  |
| xst | INFO | Xst:2261 - The FF/Latch <adc\_reg\_data\_6> in Unit <adc\_top\_interface\_2> is equivalent to the following 3 FFs/Latches, which will be removed : <adc\_reg\_data\_10> <adc\_reg\_data\_11> <adc\_reg\_data\_14> |  |